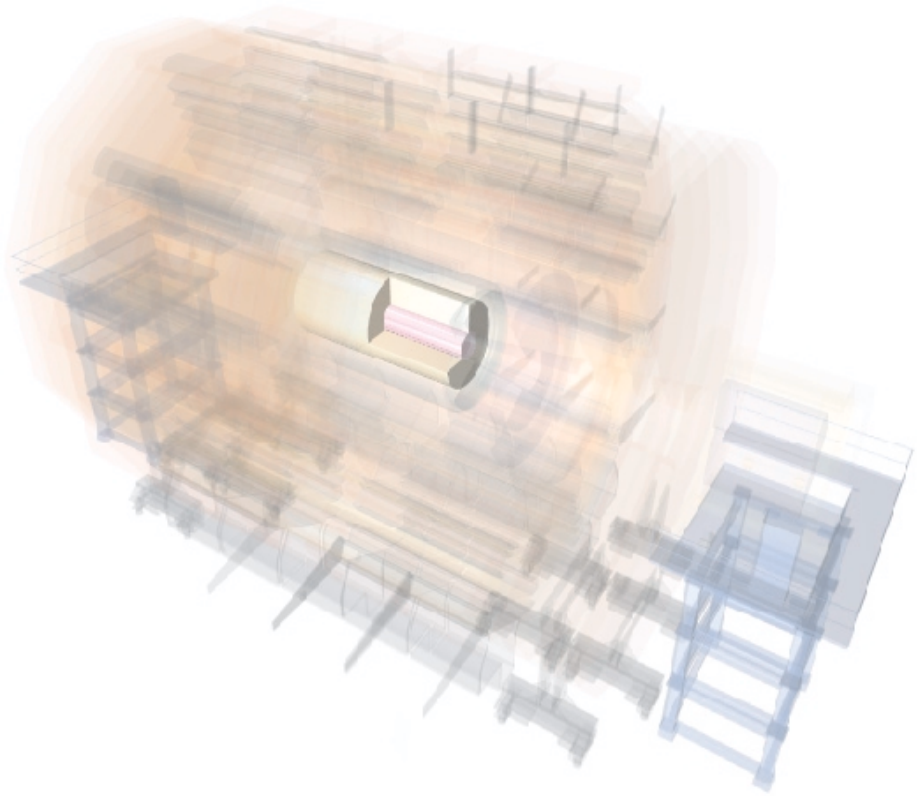
# The CMS Silicon Strip Tracker
## and its Electronic Readout



Markus Friedl · Dissertation · May 2001

Dissertation


# The CMS Silicon Strip Tracker and its Electronic Readout

presented in partial fulfillment of the requirements
for the degree Doctor of Technical Sciences
in the Department of Electrical Engineering
of the Vienna University of Technology

by

DI Markus Friedl

Belvederegasse 19/8
A-1040 Vienna
Austria
Markus.Friedl@cern.ch
Matr.No. 9126571

reviewed by

Univ.-Prof. Dr. Wolfgang Fallmann
Institute of Industrial Electronics and Material Science, Vienna University of Technology

Univ.-Doz. DI Dr. Manfred Krammer
Institute of High Energy Physics, Austrian Academy of Sciences

Vienna, May 2001

Available at http://cern.ch/friedl

# Preface

***If you understand everything, you must be misinformed.***
Japanese Proverb

Basic research in the field of high energy physics is mainly motivated by the curiosity of mankind. It does not make direct economical profit, but one may call it a cultural achievement similar to arts. General research is often reversely argumented by technological spin-offs, e.g. the World Wide Web, which originated at CERN, but there is more than meets the eye.

In fact, there are future benefits which are unpredictable at the time of discovery. When the electron was found, nobody thought about its application in television sets. Who knows what current high energy physics will bring us in the distant future?

This thesis contributes to a basic research project in particle physics. It is embedded in the Compact Muon Solenoid (CMS), a detector at the Large Hadron Collider (LHC) machine at CERN, which will be a powerful experimental tool for high energy physicists. The work is focussed on technological aspects of the CMS Silicon Strip Tracker and the evaluation of prototype readout components.

But experimental results are meaningless if not put into the right context. Thus, approximately half of this thesis is dedicated to an introduction to LHC, the principle of silicon particle detectors, the CMS experiment and especially its Silicon Strip Tracker. Despite of the above citation, I hope that the basic concepts of high energy physics experiments and the CMS Silicon Strip Tracker in particular will be conveyed.

In 1998, I began to work on the silicon detector as a member of the CMS collaboration. Since I am an Electrical Engineer, my personal emphasis has been laid upon the electronic readout, which is quite a challenging task in the LHC environment.

All of the tests described within this thesis were performed by the CMS Tracker and Electronics II groups at HEPHY [1]. In most cases, I was the main contributor to hardware and software preparation, conducted the experiments and analyzed the data.

Markus Friedl May 2001

# Abstract

The Large Hadron Collider (LHC) at CERN (Geneva, CH) will be the world's biggest accelerator machine when operation starts in 2006. One of its four detector experiments is the Compact Muon Solenoid (CMS), consisting of a large-scale silicon tracker and electromagnetic and hadron calorimeters, all embedded in a solenoidal magnetic field of 4 T, and a muon system surrounding the magnet coil. The Silicon Strip Tracker has a sensitive area of 206 $m^2$ with 10 million analog channels which are read out at the collider frequency of 40 MHz. The building blocks of the CMS Tracker are the silicon sensors, APV amplifier ASICs, supporting front-end ASICs, analog and digital optical links as well as data processors and control units in the back-end. Radiation tolerance, readout speed and the huge data volume are challenging requirements.

I have modelled the charge collection in silicon detectors which is discussed as well as the concepts of readout amplifiers with respect to the LHC requirements, including the deconvolution method of fast pulse shaping, electronic noise constraints and radiation effects.

Moreover, I performed extensive measurements on prototype components of the CMS Tracker and different versions of the APV chip in particular. I contributed to the construction of several detector modules, characterized them in particle beam tests and quantified radiation induced effects on the APV chip and on silicon detectors. In addition I evaluated a prototype of the analog optical link and the analog performance of the back-end digitization unit.

The results are very encouraging, demonstrating the feasibility of the CMS Silicon Strip Tracker system and motivating progress towards the construction phase.

**Keywords:** silicon detector, strip detector, tracker, charge collection, front-end, readout, electronics, amplifier, deconvolution, radiation damage, APV, optical link, LHC, CMS, CERN

# Kurzfassung

Der Large Hadron Collider (LHC) am CERN (Genf, CH) wird 2006 als weltweit größter Beschleuniger in Betrieb gehen. Eines seiner vier Detektor-Experimente ist das Compact Muon Solenoid (CMS), bestehend aus einem großen Silizium-Spurendetektor sowie elektromagnetischen und hadronischen Kalorimetern, die in einem axialen Magnetfeld von 4 T eingeschlossen sind, und einem außenliegenden Myon-Detektor. Der Silizium-Streifendetektor hat eine sensitive Fläche von 206 $m^2$ mit 10 Millionen Kanälen, die mit der Beschleuniger-Frequenz von 40 MHz ausgelesen werden. Die Bestandteile des CMS-Spurendetektors sind Silizium-Sensoren, APV-Verstärker-Chips und weitere ASICs im Bereich der Detektoren, analoge und digitale optische Übertragungsstrecken sowie Datenprozessoren und Steuereinheiten im Kontrollraum. Strahlungsfestigkeit, Auslesegeschwindigkeit und das enorme Datenvolumen stellen große Herausforderungen an die Elektronik.

Ich habe die Ladungssammlung in Siliziumdetektoren modelliert, die zusammen mit den Grundlagen von Ausleseverstärkern hinsichtlich der Rahmenbedingungen im LHC diskutiert wird. Dies beinhaltet unter anderem die Deconvolution-Methode der schnellen Pulsformung, den Einfluß des elektronisches Rauschens und strahlungsinduzierte Effekte.

Weiters habe ich ausführliche Messungen an Prototyp-Komponenten des CMS-Spurendetektors und insbesondere an verschiedenen Versionen des APV-Chips durchgeführt. Ich habe am Zusammenbau mehrerer Silizium-Detektormodule mitgewirkt, diese in einem Teilchenstrahl getestet und die Auswirkungen von intensiver Strahlung auf den APV-Chip und auf Silizium-Detektoren quantifiziert. Weiters habe ich einen Prototyp der analogen optischen Übertragungsstrecke evaluiert sowie die analogen Eigenschaften der für den Kontrollraum vorgesehenen Digitalisierungseinheit gemessen.

Die Ergebnisse sind sehr überzeugend, bestätigen das Konzept des CMS-Silizium-Streifendetektors und motivieren den Übergang zur Konstruktionsphase.

**Stichworte:** Siliziumdetektor, Streifendetektor, Spurendetektor, Ladungssammlung, Auslese, Elektronik, Verstärker, Strahlungsschäden, APV, Optoelektronik, LHC, CMS, CERN

# Contents


**1 Introduction** **9**
- 1.1 LHC . . . 9
- 1.2 Physics Motivation . . . 10
- 1.3 CMS Detector Layout . . . 11

**2 Silicon Sensors** **14**
- 2.1 Energy Loss . . . 14
- 2.2 Charge Collection . . . 17
- 2.3 Radiation Damage . . . 23
  - 2.3.1 Doping Concentration . . . 25
  - 2.3.2 Leakage Current . . . 26
  - 2.3.3 Charge Collection Efficiency . . . 28
- 2.4 Detector Geometry . . . 28
  - 2.4.1 Strips . . . 28
  - 2.4.2 Pixels . . . 30
- 2.5 Lorentz Shift . . . 31
- 2.6 Readout Electronics . . . 32
  - 2.6.1 Coupling . . . 32
  - 2.6.2 Amplifier . . . 33
  - 2.6.3 Deconvolution . . . 35
  - 2.6.4 Noise . . . 36
  - 2.6.5 Radiation Damage . . . 38

**3 CMS Tracker System** **40**
- 3.1 Pixel Detector . . . 41
- 3.2 Strip Detector . . . 44

**4 Strip Tracker Electronics** **49**
- 4.1 APV . . . 51
  - 4.1.1 APV25 Circuit Details . . . 52
    - 4.1.1.1 Preamplifier and Shaper . . . 53
    - 4.1.1.2 Pipeline . . . 54
    - 4.1.1.3 APSP . . . 55
    - 4.1.1.4 Multiplexer and Output Buffer . . . 57
    - 4.1.1.5 Internal Calibration . . . 59
  - 4.1.2 APV25 Output . . . 62
- 4.2 Front-End Electronics . . . 63

4.2.1 APVMUX . . . 63
4.2.2 PLL-Delay . . . 64
4.2.3 DCU . . . 65
4.3 Optical Links . . . 66
4.3.1 Analog Optical Link . . . 67
4.3.2 Digital Optical Link . . . 68
4.4 Back-End Electronics . . . 68
4.4.1 TTC System . . . 68
4.4.2 FEC and CCU . . . 68
4.4.3 FED . . . 69

**5 Experimental Results** **72**
5.1 APV Tests . . . 72
5.1.1 Hardware Setup . . . 72
5.1.1.1 APV Hybrid and Repeater . . . 73
5.1.1.2 APV Sequencer . . . 74
5.1.1.3 VME-$I^2C$ . . . 75
5.1.1.4 VME-ADC . . . 76
5.1.1.5 Module Test Setup . . . 76
5.1.1.6 Cooling Box . . . 77
5.1.2 Software . . . 78
5.1.2.1 DAQ and Analysis Software . . . 78
5.1.2.2 Slow Control Software . . . 81
5.1.3 APV6 Multiregion Module Beam Test (June 1998) . . . 81
5.1.4 APV25 Laboratory Tests (2000/2001) . . . 85
5.1.4.1 Calibration and Noise . . . 85
5.1.4.2 Source Test . . . 86
5.1.5 APV6/APV25 Beam Tests (May/December 2000) . . . 88
5.1.5.1 Setup . . . 88
5.1.5.2 Detector Module Performance . . . 89
5.1.5.3 High Intensity . . . 93
5.1.5.4 Multi-Peak Mode . . . 97
5.1.6 APV25 Irradiation (December 2000) . . . 99
5.1.6.1 Setup . . . 99
5.1.6.2 Measurement Procedure . . . 99
5.1.6.3 Digital SEUs . . . 101
5.1.6.4 Analog SEUs . . . 104
5.1.6.5 Other Results . . . 106
5.1.6.6 CMS Prediction . . . 107
5.1.7 APVMUX Test (February 2001) . . . 107
5.1.7.1 Calibration and Noise . . . 108
5.1.7.2 Crosstalk . . . 108
5.1.8 APV25 Magnetic Field Test (March 2001) . . . 110
5.2 Analog Optical Link Tests . . . 113
5.2.1 Analog Optical Link Laboratory Tests (September 1999) . . . 113
5.2.2 Laser Magnetic Field Test (March 2001) . . . 116
5.3 FED Evaluation (April 2001) . . . 120

**6 Summary** **122**
6.1 Silicon Detector Model . . . . . 122
6.2 APV Laboratory Tests . . . . . 122
6.3 Beam Tests . . . . . 123
6.4 Other Tests . . . . . 123
6.5 Outlook . . . . . 123

Appendix

**A Acknowledgements** **124**

**B Abbreviations and Symbols** **125**

**C Bibliography** **129**

**D Curriculum Vitae** **134**
D.1 List of Experiments . . . . . 135
D.2 List of Publications . . . . . 136

# Chapter 1

# Introduction

Large-scale accelerators are measuring devices for particle physicists. By the collision of highly energetic beams, a variety of particles is created which are not found in nature today. The enormous energy density provided by such colliders is used to artificially rebuild the conditions of the young universe shortly after the big bang. The interaction between theoretical prediction and experimental measurement led to a solid foundation of particle physics known as the "Standard Model" (SM).

The world's largest accelerator complex is located at CERN [2], which was founded after World War II to reunite Europe in the field of particle physics research and development. Even today, it is a political symbol of close collaboration between people from various nations, now including also non-European countries such as the USA, China or India. Only such an international cooperation allows to realize large-scale projects which a single nation could not afford.

## 1.1 LHC

Still numerous questions arising from the Standard Model could not be answered by previous accelerators due to energy limitations, motivating the development of an even bigger, new machine. The LHC (Large Hadron Collider) at CERN is an unprecedented project opening new perspectives in high energy physics. It is the successor of the LEP (Large Electron Positron) collider and has no comparable counterpart worldwide. Currently (2001), the LEP collider is being dismounted, and parts of LHC and its experiments are already under assembly. In 2006, the construction will be finished and the experiments will be taking data for about 10 years.

The LHC will reuse the LEP ring tunnel with 27 km circumference, yet it will provide much higher particle energies because collision partners are protons on protons (and alternatively lead ions) instead of electron/positron pairs. While LEP was designed for a center of mass energy of 200 GeV, LHC will reach 14 TeV with protons and 1312 TeV with lead ions. Furthermore, the LHC bunch crossing (bx) frequency of 40 MHz (corresponding to 25 ns) will be approximately thousand times higher compared to LEP. At average, every bunch crossing will result in about 18 proton-proton collisions, generating 500 charged particle tracks. Compared to the LEP electron-positron collider, where collisions occurred rarely due to the low cross-sections of electrons and positrons, the collision rate will be almost $10^9$ times higher in LHC. Such enormous rates are necessary to acquire reasonable statistics on extremely rare particles and decay processes.

The event rate $R$ in a collider is proportional to the interaction cross-section $\sigma_{\mathrm{int}}$,

$$R = \mathcal{L}\,\sigma_{\mathrm{int}} \quad , \tag{1.1}$$

with the factor $\mathcal{L}$ called luminosity [3]. When two bunches, each containing $n$ particles, collide with the frequency $f$, the luminosity is given by

$$\mathcal{L} = f\frac{n^2}{4\pi\sigma_x\sigma_y} \tag{1.2}$$

where $\sigma_x$ and $\sigma_y$ characterize the beam spread in horizontal and vertical directions.

An overview of LEP and LHC related figures is given in tab. 1.1.

| **Machine** | **Beams** | | **Energy** [TeV] | **Luminosity** [$\mathrm{cm^{-2}\,s^{-1}}$] | **bx period** [ns] | **Collision rate** [1/s] |
|---|---|---|---|---|---|---|
| LEP | $e^+$ | $e^-$ | 0.2 | $10^{32}$ | 22000 | 1 |
| LHC | p | p | 14 | $10^{34}$ | 25 | $7.2 \cdot 10^8$ |
| | Pb | Pb | 1312 | $10^{27}$ | 125 | $5 \cdot 10^3$ |

Table 1.1: Properties of LEP and LHC. The LEP collision rate refers only to hard (i.e. central) collisions.

Four detectors will be located at the collision points along the circular LHC. These are called "experiments" and will measure the enormous number of particles arising from proton-proton collisions. The two large detectors are ATLAS (A toroidal LHC apparatus) and CMS (Compact Muon Solenoid), while the smaller experiments are LHCb (B-meson experiment) and ALICE (A Large Ion Collider Experiment).

## 1.2 Physics Motivation

The main physics goal of LHC [4] is the discovery of the Higgs boson which is anticipated by the Standard Model. Theory only provides an upper limit for its mass of about 1 TeV, while LHC will reach much higher energies. In the last period of LEP, when energies were pushed to the limits, a few possible Higgs candidates were observed suggesting a mass of about 114 GeV. Due to the extended energy range of LHC, these particles will be undoubtedly confirmed and characterized if they exist as predicted by the Standard Model. Although 40 million bunch crossings occur per second in each of the four LHC experiments, the Higgs boson is expected to appear only about once every day, yet it is enough to accumulate good statistics.

Another motivation is the Charge-Parity (CP) Violation. At an early stage, the universe was dominated by energy. While expanding and cooling down, gradually matter and anti-matter formed and became dominant. However, it is not quite clear why today's world is entirely made of matter. The CP Violation implies a distinction of the weak force, which is responsible for decay, between matter and anti-matter. This could explain today's domination of matter. First reported in the 1960s, several experiments have measured the CP violation since. However, until now, it is only possible to observe a very small effect in the decay rates of Kaon particles. The results of these experiments differ considerably, and some even suggest no violation at all. LHC will enter a new energy range, allowing to study the CP violation on B-mesons, which will show a much more distinctive effect than Kaons if CP violation exists. The LHCb experiment will be dedicated to this study.

A large field of elementary particle physics is supersymmetry (SUSY). According to this theory, particles are said to have "superpartners" (sparticles). Since they have not been observed so far, SUSY must be a broken symmetry, which means that sparticles have masses different than

their counterparts. The SUSY masses are expected in the TeV range, which makes them visible to LHC. Theory predicts at least five SUSY Higgs bosons and it can provide an explanation for the dark matter of the universe.

When colliding lead ions instead of protons, the energy density is much higher. Thus, it is expected to rebuild a very early stage of the universe called quark-gluon plasma, which may reveal different physical properties.

## 1.3 CMS Detector Layout

Fig. 1.1 shows the full CMS detector [5, 6], which is 15 m in diameter, 21.6 m long and weighs 12500 t. It relies on four principal sub-systems: A high-quality central tracking system (pink and yellow), surrounded by an electromagnetic calorimeter (green), a hermetic hadron calorimeter (purple) and finally a muon detector (red and yellow).

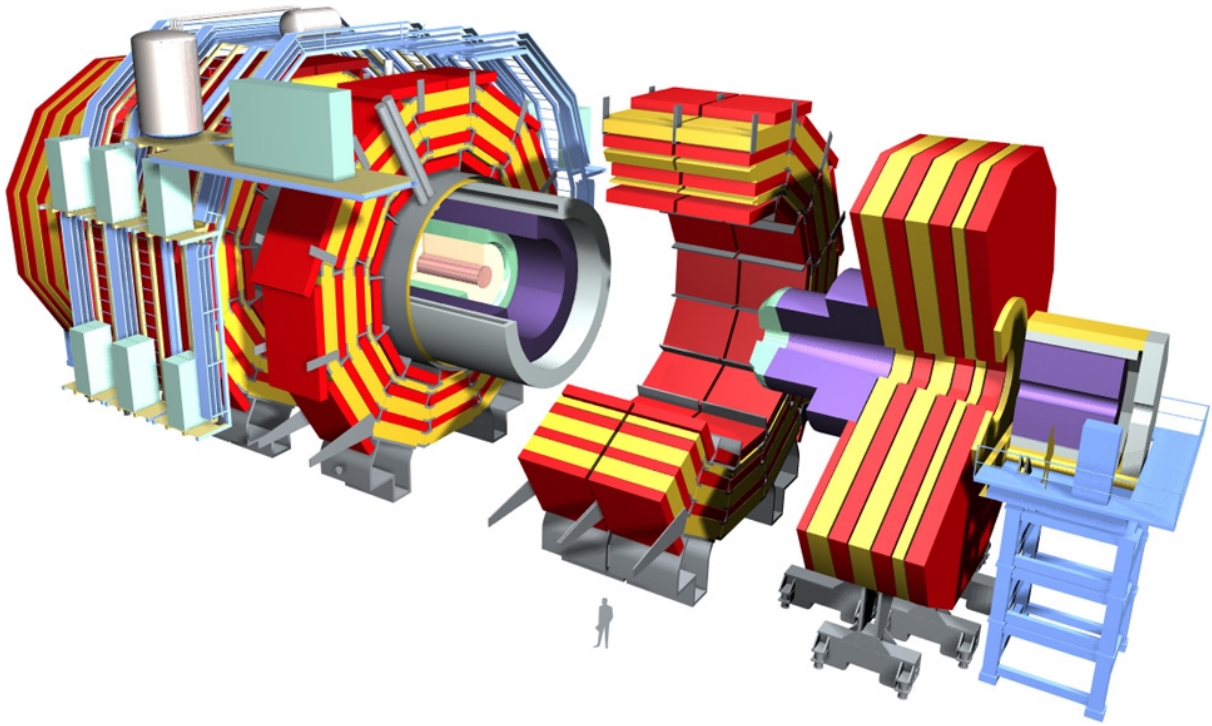


Figure 1.1: The CMS experiment at CERN.

All subsystems of the experiment are divided into a cylindrical barrel part and the two facing endcap sections. The "forward" region, shown on the scaffold to the right, is further away from the interaction point at very small angles. This arrangement gives a good coverage of almost everything arising from a collision, which is important for the reconstruction of events.

A short introduction will be given to the components of the CMS experiment from the innermost to the outermost detectors. Fig. 1.2 shows a longitudinal view of CMS, where the origin denotes the interaction point. The angle specifications on top and left are given in units of pseudorapidity $\eta$, which is defined by

$$\eta = -\ln\left(\tan\frac{\alpha}{2}\right) \quad \text{and} \tag{1.3}$$

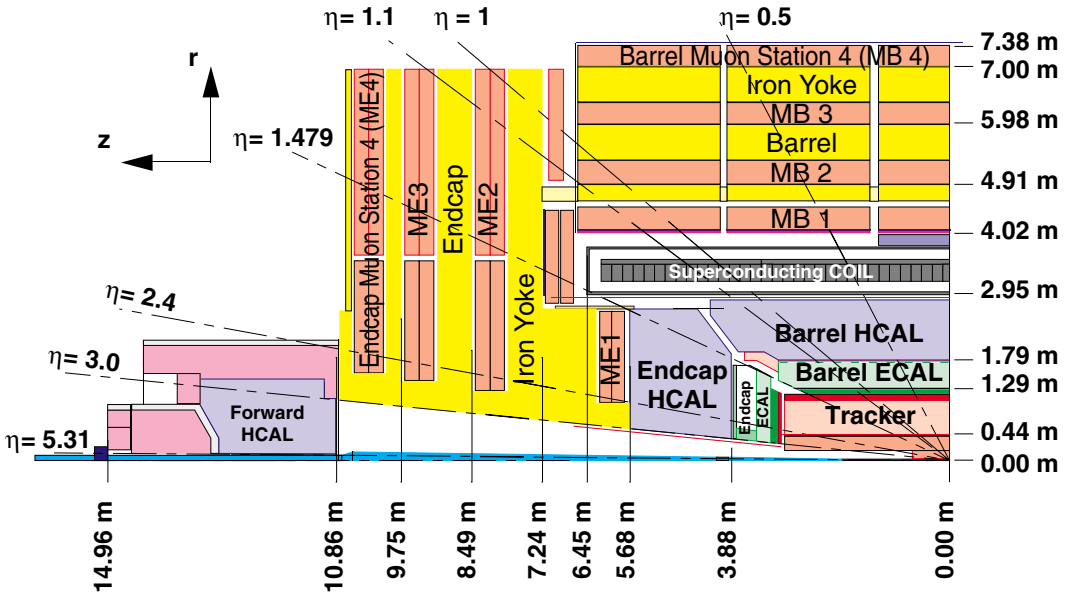



Figure 1.2: Longitudinal view of one quadrant of CMS.

$$\frac{r}{z} = \tan\alpha \quad ,$$

where $\alpha = 90°$ is perpendicular to and $\alpha = 0°$ coincides with the beam axis.

The central tracker consists of three pixel layers and ten strip layers. Its task is to measure the tracks of charged particles with a minimum of interaction. Originally, Micro-Strip Gas Chambers (MSGCs) were planned for its outer part. However, problems were repeatedly reported concerning aging and high voltage (HV) stability. Thus, the CMS Tracker community decided to build an all-silicon tracker [7, 8] instead, which now covers a sensitive area of 206 $m^2$. The Tracker, as it is the main topic of this thesis, will be discussed in detail in chapter 3.

The electromagnetic calorimeter (ECAL) consists of approximately 76000 scintillating $PbWO_4$ crystals with a depth of 23 cm (corresponding to 25 radiation lengths $X_0$) and a cross-section of $2.2 \times 2.2\,cm^2$. Electrons and photons are converted to light pulses, which are read out by silicon avalanche photodiodes. A small loss in attenuation of a few percent due to color center formation is observed from radiation. This effect can be calibrated with light injection into the crystal.

The main part of the hadron calorimeter (HCAL) is located inside the magnet, which is surrounded by a an additional small part in the central region ("tail catcher"). The central HCAL consists of a brass/scintillator sampling calorimeter. Its scintillation light is captured, wavelength shifted and guided to hybrid photodiodes. The active depth of the HCAL exceeds nine nuclear interaction lengths $\lambda_I$, corresponding to more than 99% containment of hadronic cascades. The forward part of the HCAL consists of a steel absorber with quartz fibers. Traversing charged particles produce Cherenkov light in the fibers which is guided to photomultipliers.

The calorimeters are intended for energy measurement and triggering. They are surrounded by a superconducting coil providing a solenoidal magnetic field of 4 T. The tracks of charged particles bend in this magnetic field $B$ which allows to measure the polarity of their charge $q$ and, assuming elementary charge, their momentum $p$ using the relation

$$p = q\,B\,r \quad , \tag{1.4}$$

where $r$ is the bend radius. This equation is given here in a non-relativistic form; it has to be adapted for velocities close to the speed of light like those which occur in the LHC experiments. Moreover, the polarity can be obtained by the bend orientation.

The Muon System consists of four stations in both barrel (MB1...MB4) and endcap (ME1...ME4) parts, which are integrated in the iron return yoke of the magnet. In the barrel part, each station consists of twelve layers of Drift Tube Chambers (DT). Resistive Plate Chambers (RPC) are used for bunch crossing identification and provide a cut on the muon transverse momentum at the first level trigger. In the endcap region, each station consists of six stations of Cathode Strip Chambers (CSC).

Four logic blocks make up the Trigger and Data Acquisition System. The first two stages, front-end detector electronics and first level trigger processors, are synchronous and pipelined. The first level trigger has to reduce the 40 MHz bunch crossing rate to an event rate of 100 kHz by filtering only interesting events. This trigger decision has a delay of 3.2 $\mu$s in relation to the corresponding bunch crossing. To avoid dead time, the data collected within this period must be stored in the front-end in order to pass it on after a trigger request.

The two later stages are a large switching network ("event builder") with a throughput of 500 Gbit/s and an on-line event filtering system implemented in a computer farm. These stages are made of commercial components and thus can be upgraded as technology develops.

The combined information of all detector subsystems is used for the total event reconstruction and quantification. While the silicon tracker is intended for momentum and polarity identification, the energy is measured by the calorimeters, and penetrating muons are detected in the outermost layer. The triggering information is derived from calorimeters and the muon system.

# Chapter 2

# Silicon Sensors

## 2.1 Energy Loss

The principle of solid state detectors is based on the energy loss of traversing particles. Free electron-hole pairs are generated, which move towards opposite electrodes under the influence of an electric field. The energy loss of heavy particles in matter was described by H.A.Bethe[1] and F.Bloch[2] [3].

$$-\frac{1}{\rho}\frac{dE}{dx} = 4\pi N_A r_e^2 m_e c^2 z^2 \frac{Z}{A}\frac{1}{\beta^2}\left[\frac{1}{2}\ln\left(\frac{2m_e c^2\beta^2\gamma^2 T_{\max}}{I^2}\right) - \beta^2 - \frac{\delta(\gamma)}{2} - \frac{C}{Z}\right] \tag{2.1}$$

Eq. 2.1 represents the differential energy loss per mass surface density [MeV $(\mathrm{g\,cm^{-2}})^{-1}$], where $ze$ is the charge of the incident particle, $N_A$, $Z$ and $A$ are Avogadro's number, the atomic number and the atomic mass of the material, $m_e$ and $r_e$ are the electron mass and its classical radius ($\frac{e^2}{4\pi\epsilon_0 m_e c^2}$). $T_{\max}$ is the maximum kinetic energy which is still detected in the material, $I$ is the mean excitation energy, $\beta = v/c$, $\gamma = (1-\beta^2)^{-1/2}$ and $\delta(\gamma)$ is a correction for the shielding of the particle's electric field by the atomic electrons, the density effect caused by atomic polarization. At very low incident particle energies, the basic assumption of static atomic electrons is violated, which is taken into account by the shell correction term $C$.

However, in thin layers, the deposited energy is less than expected because a fraction of the lost energy is carried off by energetic knock-on electrons (also known as $\delta$ electrons). These considerations lead to the restricted energy loss, which is expressed by an additional term in the Bethe-Bloch equation [9],

$$-\frac{1}{\rho}\frac{dE}{dx} = 4\pi N_A r_e^2 m_e c^2 z^2 \frac{Z}{A}\frac{1}{\beta^2}\left[\frac{1}{2}\ln\left(\frac{2m_e c^2\beta^2\gamma^2 T_{\mathrm{upper}}}{I^2}\right) - \beta^2\left(1+\frac{T_{\mathrm{upper}}}{T_{\max}}\right) - \frac{\delta(\gamma)}{2} - \frac{C}{Z}\right] \quad , \tag{2.2}$$

where $T_{\mathrm{upper}} = \inf(T_{\mathrm{cut}}, T_{\max})$ with $T_{\mathrm{cut}}$ depending on the material and the incident particle momentum.

[1] Hans Albrecht Bethe, *1906 in Strasbourg. Most of the time he worked with the Cornell University, interrupted by sabbaticals leading him to CERN and other research centers. For his contributions to the theory of nuclear reactions he was awarded the Nobel Prize in 1967.

[2] Felix Bloch, *1905 in Zurich, †1983 in Zurich. He was working with several universities and research centers, like Stanford and CERN. The Nobel Prize was awarded to him in 1952 for nuclear magnetic precision measurements.

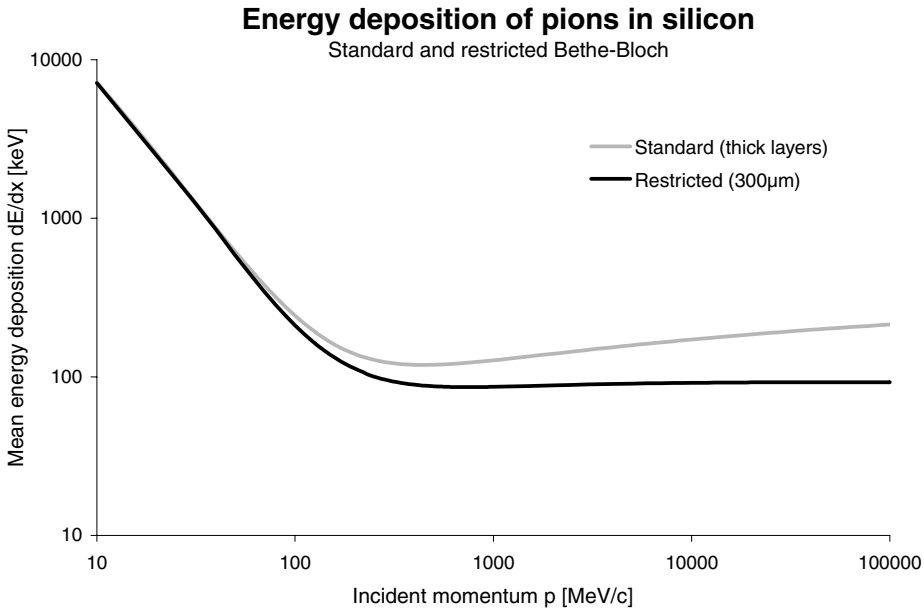



Figure 2.1: Energy deposition of pions in silicon. While the standard Bethe-Bloch theory covers thick layers, restrictions apply to thin layers as shown for 300 $\mu$m to account for energy carried off by energetic knock-on electrons.

Fig. 2.1 compares the standard Bethe-Bloch theory to the restricted form for a pion traversing 300 $\mu$m of silicon in terms of the incident particle momentum. In the low energy range, there is no difference between standard and restricted forms, since knock-on electron production is improbable. However, in the regime of a few hundred MeV/c, there is already considerable deviation: The standard theory predicts a minimum ionizing particle (MIP) at 450 MeV/c, while the restricted energy loss states 750 MeV/c. Moreover, the relativistic rise at high energies is quite flat in the restricted model due to energy carried off by knock-on electrons.

The statistical fluctuation of the energy loss in thin layers was described by L.D.Landau[3] [10]. The Landau distribution resembles a distorted normal distribution with a long upper tail due to rare, but highly ionizing knock-on electrons.

The tail of an ideal Landau distribution extends to infinite energies, which is unrealistic. In practice, the measurement range is always limited, which leads to a truncated Landau curve. As a result of its asymmetry, the mean energy loss is higher than the most probable (MP). However, the latter is much easier to obtain from measured data and therefore usually stated in experimental results. The scale factor between MP and mean is typically around 1.3 but depends on particle energy and measurement range.

With particle energies far below the MIP energy, corresponding to thick layers, knock-on electrons are improbable, the Landau tail vanishes and thus the resulting distribution is Gaussian[4].

The restricted energy loss model has been confirmed by experiments, e.g. by a dedicated

[3]Lev Davidovich Landau, *1908 in Baku (Azerbaijan), †1968 in Moscow. The work of the Soviet physicist covers all branches of theoretical physics. In 1962 the Nobel Prize was awarded to him for his pioneering theories about condensed matter, especially liquid helium.

[4]Carl Friedrich Gauss, *1777 in Braunschweig, †1855 in Göttingen (both Germany). German mathematician who worked in the fields of number theory, geometry, astronomy, and geodesy. He also introduced the bell-shaped curve known by his name which is fundamental in the description of statistical data.

test with silicon pad sensors at BNL performed in 1998 by HEPHY and MIT, where excellent agreement between measurement and theory was found [11]. Fig. 2.2 shows the most probable energy loss of pions in the range of minimum ionization in a silicon detector of 300 $\mu$m thickness.

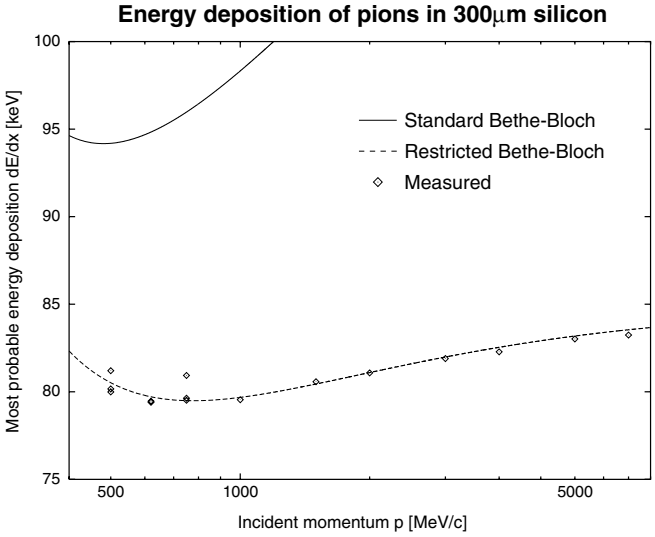



Figure 2.2: Calculated and measured most probable energy deposition of pions in a silicon detector of 300 $\mu$m thickness, compared to the standard Bethe-Bloch theory.

The energy deposited in the detector material flows into the creation of free electron-hole pairs. The number of pairs $n$ depends on the total energy loss $E_{\text{loss}}$ and the ionization energy $E_{eh}$, which is necessary for a pair production,

$$n = \frac{E_{\text{loss}}}{E_{eh}} \quad . \tag{2.3}$$

In silicon, $E_{eh} = 3.6\,\text{eV}$, which results in an most probable charge of about $n = 22000$ pairs for a MIP in 300 $\mu$m of silicon. Different values between 20000 and 25000 pairs (corresponding to a charge between $2 \times 3.2$ and 4 fC) are given in literature. Within this thesis, a number of $n = 22500$ pairs shall be defined as the MIP charge.

The measured energy loss distribution of MIPs in a typical silicon sensor (300 $\mu$m thick) is shown in fig. 2.3 in terms of the collected charge [12]. The measured data have been fitted by a Landau distribution, convoluted with a narrow normal distribution due to electronic noise and intrinsic detector fluctuations [13]. This results in a minor broadening of the shape and a slight increase of the peak position compared to pure Landau. As stated in the boxes on the right, the pure Landau MP = 22250 e, but after convolution with a Gaussian distribution of $\sigma = 3136$ e, the position of the peak = 23512 e. Since the convoluted peak is the measured property, we will implicitly refer to this value when stating experimental MP signal values.

Fig. 2.3 also illustrates why the MP is obtained much easier than the mean value: Cuts on either end do affect the mean, but not the MP. The low edge depends on the pedestal threshold, and the high edge is defined by the range of the readout electronics. Moreover, nonlinearity and saturation occur when measuring very high signals of the tail.

More experimental results, which confirm the theory of energy loss, are found in section 5.1.5.2, p. 89.

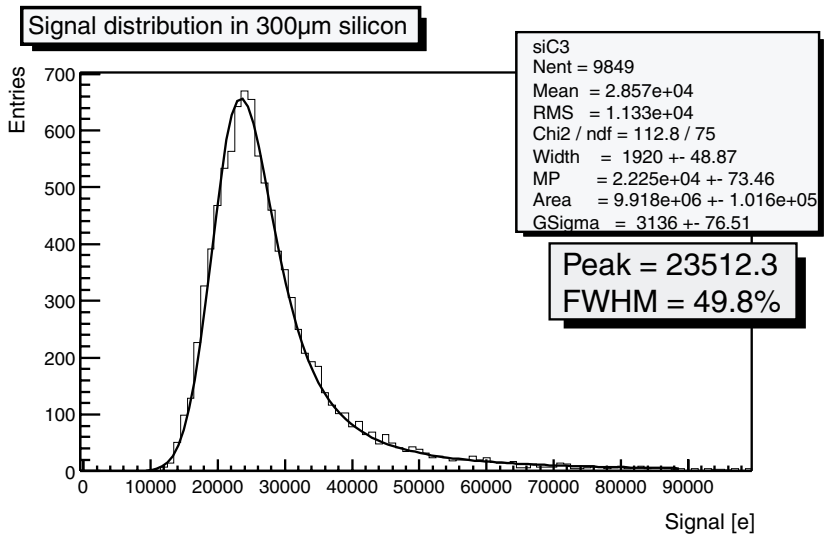



Figure 2.3: Measured MIP signal distribution in a silicon detector of 300 $\mu$m thickness.

## 2.2 Charge Collection

The ionization of particles traversing the detector leads to the creation of free electron-hole pairs as discussed in the previous section. Fig. 2.4 shows the principal layout of a solid state detector with opposite electrodes.

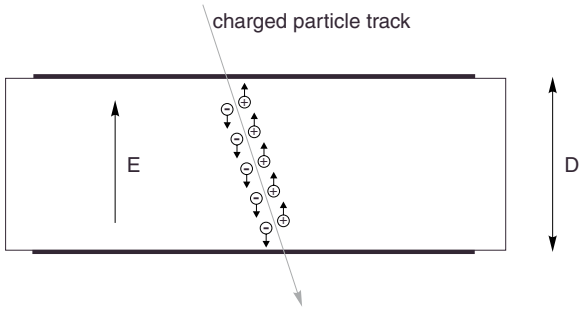



Figure 2.4: A charged particle traversing the detector generates free electron-hole pairs along its track, which are moved by the electric field.

An electric field between the electrodes is required to move these carriers according to the relation

$$v = \mu E \quad , \tag{2.4}$$

where is $v$ is the mean carrier drift velocity, $\mu$ the mobility and $E$ the electric field. The mobilities and thus drift velocities are different for electrons and holes. The linear relation of eq. 2.4 is only valid for weak electric fields; at high electric field strength, the increasing number of collisions of the carriers with the crystal lattice finally leads to saturation of the average velocity. For silicon, empirical functions have been found for electrons and holes [14, 15],

$$v_e \quad = \quad \frac{\mu_e E}{\sqrt{1 + \left(\frac{\mu_e E}{v_{e,\,\mathrm{sat}}}\right)^2}} \quad \text{and} \tag{2.5}$$

$$v_h = \frac{\mu_h E}{1 + \frac{\mu_h E}{v_{h,\,\mathrm{sat}}}} \quad ,$$

where $v_{h,\,\mathrm{sat}}$ and $v_{h,\,\mathrm{sat}}$ denote the saturation velocities, which are in the order of $10^7$ cm/s. These general relations for electron and hole velocities are graphically shown in fig. 2.5.

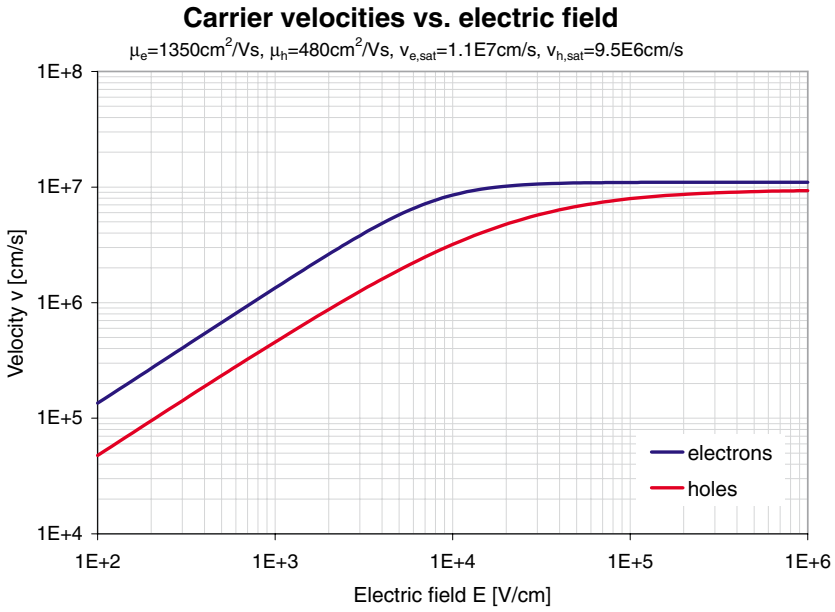



Figure 2.5: Electron and hole velocities vs. the electric field strength in silicon.

While the charges move inside the detector bulk, a current is induced in the electrodes, no matter whether the carriers finally reach the electrodes or not. This current $i$ is proportional to the sum of all carrier velocities [16],

$$i = \frac{e}{D}\left(\sum v_e + \sum v_h\right) \quad , \tag{2.6}$$

with the elementary charge $e$ and the detector thickness $D$. The integrated current gives the total collected charge $Q_c$, which is usually measured with integrating and thus charge-sensitive amplifiers,

$$Q_c = \frac{e}{D}\int\left(\sum v_e + \sum v_h\right) dt \quad . \tag{2.7}$$

After the generation of a free electron-hole pair, the electron moves to the positive electrode while the hole moves to the negative. If no charges are trapped, the sum of the distance they travel equals the detector thickness, regardless of their initial position. Thus, the integral term in eq. 2.7 equals the detector thickness multiplied by the number of pairs $n$, and the total collected charge is

$$Q_c = n\,e \quad . \tag{2.8}$$

The collected charge is stated in terms of electrons, which might mislead to the false conclusion that only the electrons contribute to the charge measured at the electrode. In fact, both electrons and holes are responsible for the charge collection in equal parts, since on average both carriers travel through half of the detector if no charge trapping occurs.

In usual silicon detectors, virtually all charges finally reach the electrodes. After heavy irradiation however, charge traps emerge such that the mean travel distance shrinks. In other solid state detector materials, such as diamond [17] or gallium arsenide [18], charge traps are always present, resulting in a mean pair travel distance less than the detector thickness. The charge collection efficiency $\eta_c$ can thus be expressed by the mean travel distance, which is also called "charge collection distance" $d_c$, divided by the detector thickness,

$$\eta_c = \frac{d_c}{D} \quad . \tag{2.9}$$

Depending on the sensor material, the electric field can be homogeneous or not. Diamond detectors merely consist of a thin film with ohmic contacts on both sides. An applied voltage results in a homogeneous field between the electrodes. With silicon however, it is impossible to operate a detector this way, because the intrinsic number of free carriers due to thermal excitation would be orders of magnitude higher than the expected detector signal. Thus, one either has to cool down the sensor to very low temperature or introduce a reverse-biased pn-junction, which is obviously more practical.

A junction is introduced by doping with acceptors and donors resulting in zones of p and n types. Starting with a homogeneously doped material, a thin layer with a high doping density of the other type is applied onto the surface, resulting in a pn-junction. On the opposite surface, which is known as backplane, the bulk type doping is enhanced to get a good ohmic contact. Fig. 2.6 shows the schematic layout of a silicon detector based on n-type bulk material, which is mostly used. Once the junction is under reverse bias, all free carriers in the bulk are drained by the electric field. The thickness of the implants with high doping concentration ($p^+$ and $n^+$) is in the order of a micrometer, so that the difference between bulk and total detector thickness is negligible.

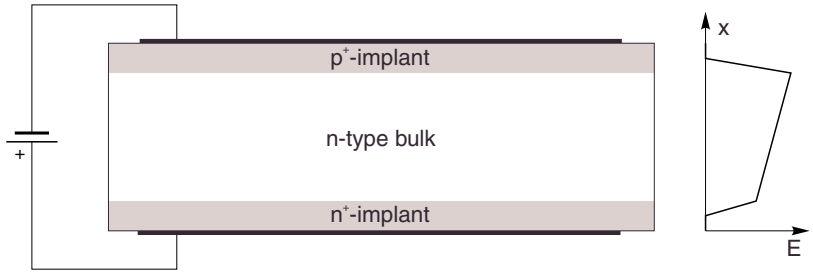



Figure 2.6: Schematic cross-section of a silicon detector with implant thicknesses not to scale. The electric field results from a bias voltage above the depletion voltage.

The bulk donor (or acceptor) density $N$ can be obtained from its resistivity $r$. In the case of an n-type bulk the relation is

$$N = \frac{1}{r\, e\, \mu_e} \quad . \tag{2.10}$$

The electric properties in a one-dimensional detector model are illustrated by fig. 2.7. Backplane and implant thicknesses are neglected and an abrupt junction is assumed.

When the pn-junction is fully depleted (i.e. there are no free carriers in the bulk), only the core excess charges of donors and acceptors remain, such that the charge densities of bulk $\rho_{\mathrm{bulk}}$ and $p^+$ implant $\rho_{\mathrm{p}}$ are

$$\rho_{\mathrm{bulk}} = e\, N_{\mathrm{bulk}} \quad \text{and} \quad \rho_{\mathrm{p}} = -e\, N_{\mathrm{p}} \quad . \tag{2.11}$$

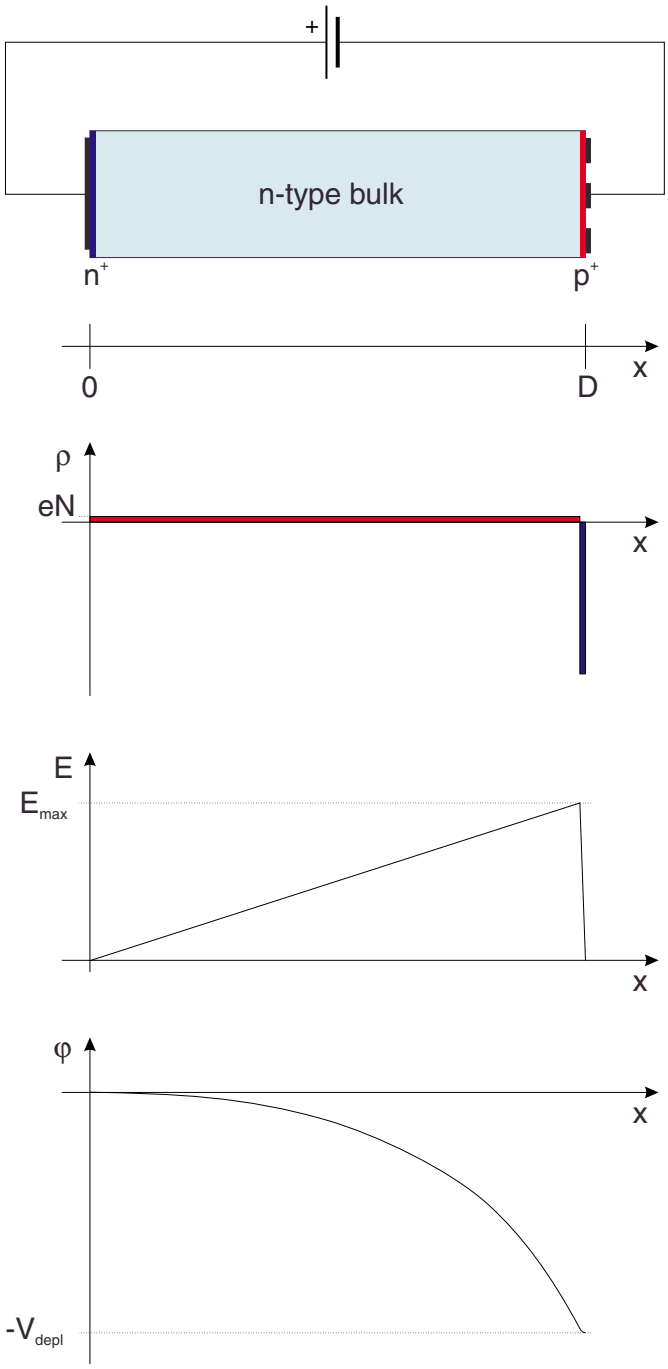



Figure 2.7: Charge density, electric field and potential in a one-dimensional model of a silicon detector at full depletion.

The bulk charge density is constant over the full width of the bulk. Since the global charge must be balanced in a steady state, positive and negative charges have to match. This condition is leads to the width $d_p$ of constant non-zero implant charge density which is equal to the bulk width but scaled down by the ratio of doping concentrations,

$$d_p = D\frac{N_{\text{bulk}}}{N_{\text{p}}} \quad . \tag{2.12}$$

The charge density $\rho$ can be obtained by the Poisson equation

$$\frac{dE}{dx} = \frac{\rho}{\epsilon} \tag{2.13}$$

with the dielectric constant $\epsilon$. In the case of full depletion, the electric field is of triangular shape, rising from zero at the backplane ($x = 0$) to its maximum at the junction ($x = D$). In the implant, the field quickly drops to zero again. The maximum electric field $E_{\text{max}}$ is given by

$$E_{\text{max}} = \frac{eN_{\text{bulk}}D}{\epsilon} \quad . \tag{2.14}$$

The relation

$$\frac{d\varphi}{dx} = -E \tag{2.15}$$

defines the electric potential $\varphi$. The potential difference between backplane and implant electrodes is the voltage $V$ applied to the detector. At full depletion, $V_{\text{depl}}$ is given by

$$V_{\text{depl}} = \frac{eN_{\text{bulk}}D^2}{2\epsilon} = \frac{D^2}{2r\mu_e\epsilon} \quad . \tag{2.16}$$

If the applied voltage is higher than the depletion voltage, a constant offset adds to the electric field as shown in fig. 2.6. With $V \gg V_{\text{depl}}$, the electric field can be approximately considered constant. When the applied voltage is below full depletion, the field does not extend over the whole bulk. With its maximum still at the junction, only a fraction of the sensor is depleted. Obviously, the charge collection is inefficient in that case, since the carriers do not move outside the electric field. The width of the depletion zone, or collection distance $d_c$, is given by

$$d_c = D\sqrt{\frac{V}{V_{\text{depl}}}} \quad . \tag{2.17}$$

Thus, the efficiency of a silicon detector is given by

$$\begin{aligned} \eta_c &= \sqrt{\tfrac{V}{V_{\text{depl}}}} \quad \text{for } 0 \le V \le V_{\text{depl}} \\ \eta_c &= 1 \qquad\qquad\quad \text{for } V \ge V_{\text{depl}} \quad . \end{aligned} \tag{2.18}$$

Fig. 2.8 compares the theoretical efficiency (eq. 2.18) to measurement [12].

In a homogeneous electric field, the carrier velocities are constant. Initially all carriers move towards the electrodes and gradually they are drained at the electrodes until all charges are gone. As the mobilities of electrons and holes differ, the current waveform is a superposition of two triangles of the same area, but different slope.

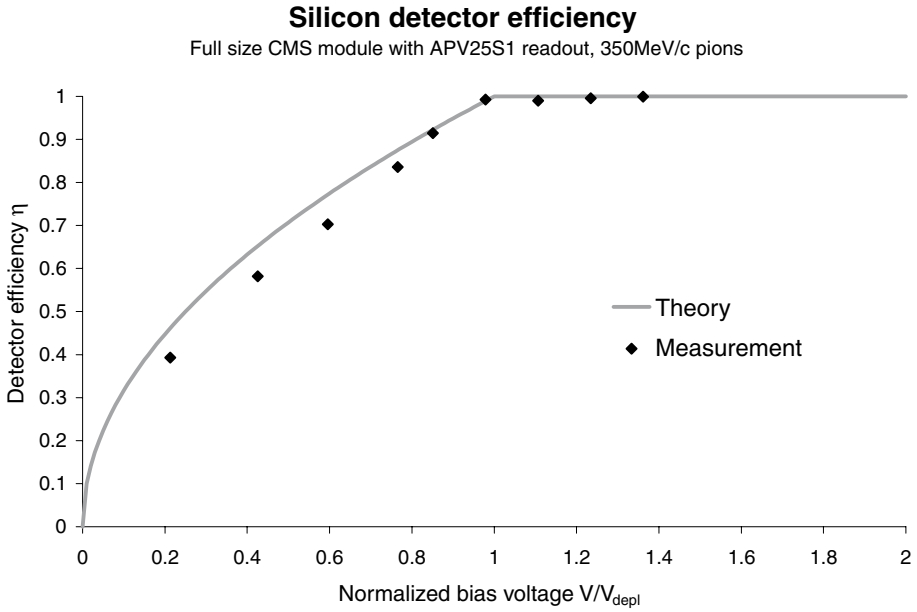



Figure 2.8: Theoretical and measured efficiency of a silicon detector. While theory suits well at depletion and above, it does not perfectly describe the low voltage regime.

In silicon detectors however, the behavior is different because the electric field depends on the position and moreover, the carrier velocities are on the edge of saturation. For a better understanding of the influence of the various parameters, the current waveform has been simulated [19, 20] based on the above model including the nonlinear velocities (eq. 2.5). The movement and resulting currents of both electrons and holes are calculated in finite time steps.

Fig. 2.9 shows the current contributions of electrons and holes in a standard silicon detector at $V_{\mathrm{depl}}$ and at $2V_{\mathrm{depl}}$. Neglecting the nonlinear velocities and the quantization of the carriers, it can be shown that the electron component follows an exponential decay at full depletion. A single electron starting at the junction ($x = D$) moves according to

$$D - x = \int v\, dt \quad . \tag{2.19}$$

Substituting the velocity with eq. 2.4 and using a linear dependence of the electric field on the position, one gets the differential equation

$$-\frac{d}{dt}x = \frac{\mu_e E_{\max}}{D}x \tag{2.20}$$

with the solution

$$x(t) = De^{-\frac{\mu_e E_{\max}}{D}t} \quad , \tag{2.21}$$

using the initial condition $x = D$. In the case of twice the depletion voltage as shown in the insert of fig. 2.9, the current shapes are approximately linear since the electric field is almost constant.

Fig. 2.10 shows the sum current of detectors with various thicknesses at their respective depletion voltages, which scale with the square of the thickness (eq. 2.16). The current waveforms approximately scale with the thickness. Although the distances, which the carriers have to travel, are farther, the higher electric field results in faster movement. If the linear relationship between

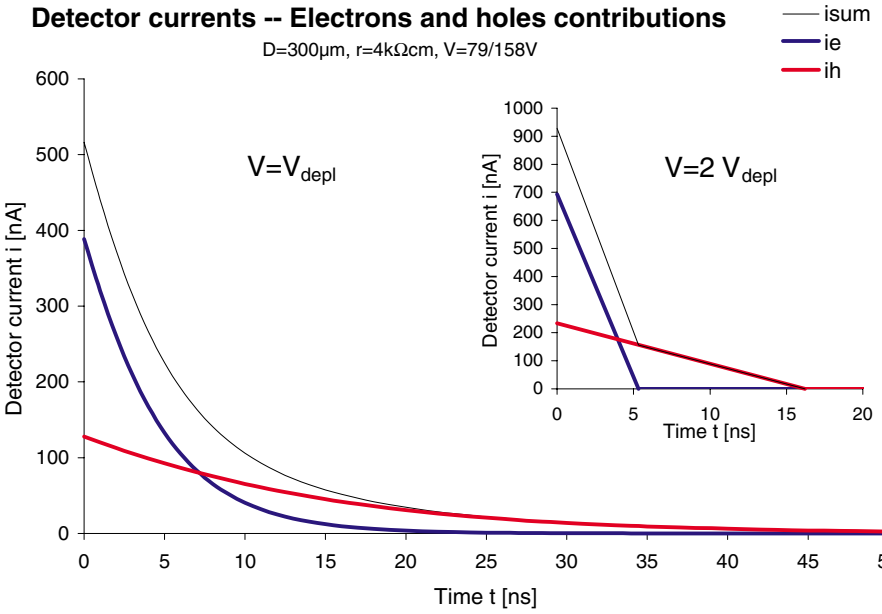



Figure 2.9: Electron and hole currents induced by a MIP in a standard silicon detector ($D = 300\,\mu$m, $r = 4\,\mathrm{k\Omega cm}$) at the depletion voltage and at $V = 2V_{\mathrm{depl}}$.

electric field and carrier velocities (eq. 2.4) held, the collected charge would exactly scale with the detector thickness at the respective depletion voltage. The overall drift time $t_{\mathrm{drift}}$ is given by

$$t_{\mathrm{drift}} = \frac{D}{v} \quad . \tag{2.22}$$

The velocity will be substituted with the integral average of eq. 2.4 over $x$,

$$v = \frac{1}{D}\int_0^D \mu E(x)dx \quad . \tag{2.23}$$

With the linear dependence of the electric field on the position, we get

$$t_{\mathrm{drift}} = \frac{D^2}{\int_0^D \frac{\mu N_{\mathrm{bulk}}}{\epsilon} x\, dx} = \frac{2\epsilon}{\mu e N_{\mathrm{bulk}}}, \tag{2.24}$$

which is independent of the thickness. Although the maximum electric field in silicon detectors of 300 to 500 $\mu$m touches the saturation region of the carrier velocities, the nonlinear influence is not yet dominant, as seen in fig. 2.10. Thus, the benefit of silicon detectors thicker than the canonical 300 $\mu$m is an approximately proportionally higher signal output.

## 2.3 Radiation Damage

The total fluences of photons, neutrons and charged hadrons expected in the CMS experiment over the scheduled 10 years of LHC operation is shown in fig. 2.11. $z$ is the distance from the vertex along the beam axis, while the parameter is the radius $r$. In the region of the CMS Tracker, charged hadrons are dominant, most of which are pions with a momentum below

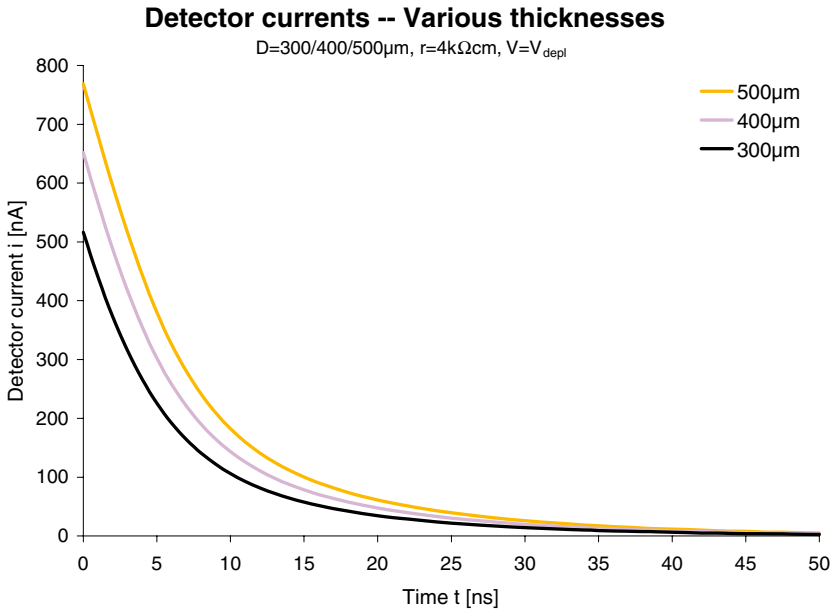



Figure 2.10: Currents induced by a MIP in silicon detectors ($r = 4\,\mathrm{k\Omega cm}$) of various thicknesses ($D = 300, 400, 500\,\mu\mathrm{m}$) at their depletion voltages ($V_{\mathrm{depl}} = 79, 141, 220\,\mathrm{V}$).

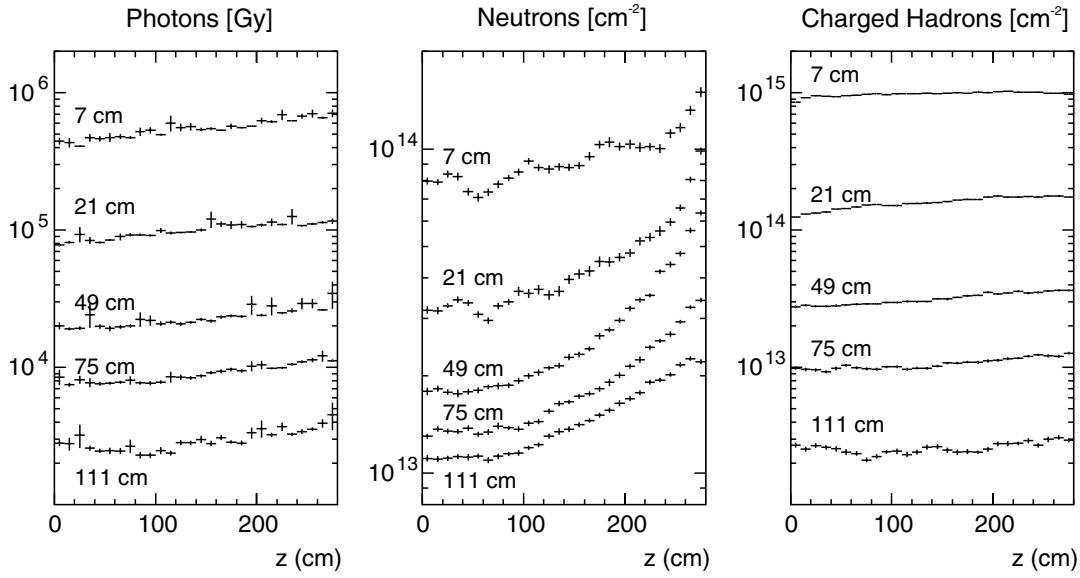



Figure 2.11: The expected radiation fluences of photons, neutrons and charged hadrons in the CMS experiment over 10 years of operation as a function of the distance $z$ from the collision point along the beam axis and the radius $r$.

1 GeV/c. The innermost layer of the strip tracker ($r = 27.7\,\mathrm{cm}$) has to deal with a total fluence of less than $2 \cdot 10^{14}\,\mathrm{particles\,cm^{-2}}$.

Radiation effects in silicon are usually normalized to an equivalent fluence of 1 MeV neutrons. With few exceptions, the damage of pions, protons and neutrons at various energies can be scaled using the Non Ionizing Energy Loss (NIEL) values [21].

Intense irradiation causes three effects in silicon, which have been studied extensively by the CERN RD48 collaboration [22]. The doping concentration changes, the leakage current increases proportional to the fluence and the charge collection efficiency decreases due to charge trapping.

### 2.3.1 Doping Concentration

With irradiation, both donors are removed and acceptor-like defects are generated throughout the bulk. This effect leads to a decrease of the effective bulk doping concentration

$$N_{\mathrm{bulk}} = |N_D - N_A| \quad , \tag{2.25}$$

and eventually, there are equal numbers of donors and acceptors. The effective doping concentration is zero then and the silicon behaves as if it were intrinsic. This state is known as the inversion point. With further irradiation, the acceptors begin to dominate, and the bulk material is now effectively of p-type. This implies that the pn-junction has moved to the backplane side. As the depletion voltage scales with the bulk doping concentration (eq. 2.16), the bias voltage has to be adjusted during the irradiation process to ensure full depletion. Initially, the depletion voltage decreases to theoretically zero at the depletion point, and then rises with the effective bulk doping concentration. The fluence needed for inversion depends on the initial doping concentration. High-resistivity sensors have a low initial donor density and reach the inversion point with less fluence than those of low resistivity.

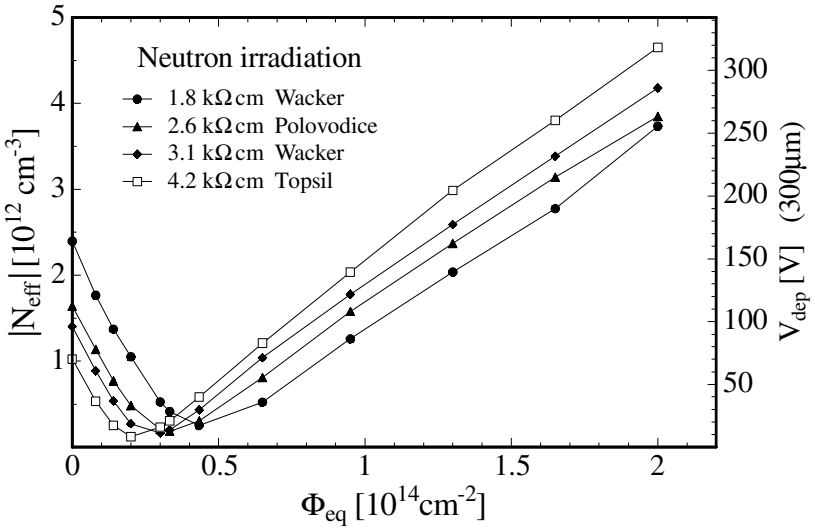



Figure 2.12: Effective doping concentration and depletion voltage of silicon detectors vs. 1 MeV neutron equivalent fluence [22]. The fluence needed to reach the inversion point depends on the initial resistivity.

Fig. 2.12 shows the development of the depletion voltage for silicon detectors of various initial resistivities and manufacturers over the equivalent fluence $\Phi_{\mathrm{eq}}$ of 1 MeV neutrons. Various

attempts have been made on flattening the $dN/d\Phi$ slope, which is a parameter describing the radiation hardness of the material. While carbon contamination was identified to have a bad influence on the radiation induced doping concentration change, oxygen enriched silicon detectors tolerate a three times higher fluence of charged hadrons compared to standard material. However, no difference was observed regarding neutrons. The comparison of the doping concentration development between standard silicon and oxygen enriched material is shown in fig. 2.13.

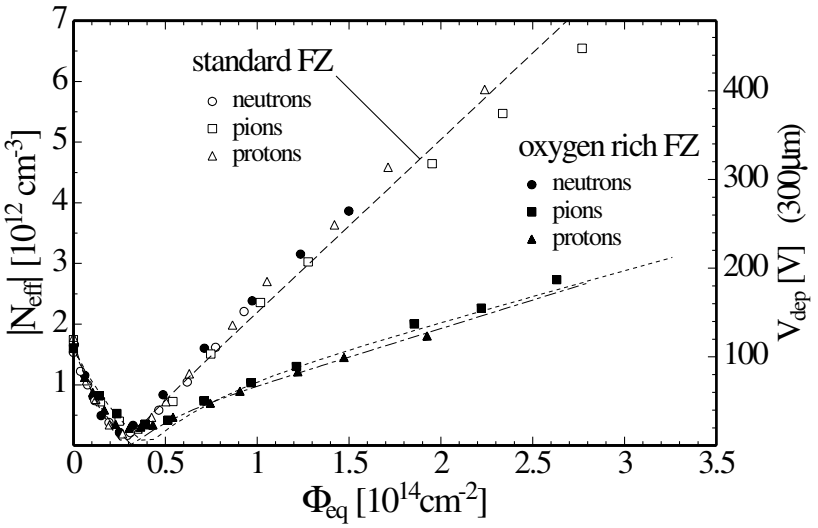



Figure 2.13: Dependence of the effective bulk doping concentration on the 1 MeV neutron equivalent fluence for standard and oxygen enriched silicon [22].

The influence of inversion on the particle induced current has been modelled with the simulation discussed in section 2.2, p. 17, neglecting the efficiency decrease due to radiation. At the same effective doping concentrations before and after inversion, the depletion voltages are equal, but the triangular shape of the electric field flips, since the pn-junction moves from the readout to the backplane side. Thus, the current contributions of individual carriers are quite different, but nevertheless the sum currents of both electrons and holes are the same before and after inversion. Fig. 2.14 demonstrates this amazing feature by investigating a single electron-hole pair, five pairs and the real case, a large number of charge carriers.

### 2.3.2 Leakage Current

Radiation damage also causes an increase in the detector current $I$, which is strictly proportional to the equivalent fluence $\Phi_{\text{eq}}$ and the sensitive volume $V$,

$$\Delta I = \alpha \, \Phi_{\text{eq}} \, V \quad , \tag{2.26}$$

where $\alpha$ is the current related damage rate, which is independent on material type and resistivity. The leakage current in silicon detectors is strongly temperature dependent according to

$$I \propto T^2 \, e^{-\frac{E_g}{2kT}} \quad , \tag{2.27}$$

where $T$ is the operating temperature, $E_g$ the band gap and $k$ the Boltzmann constant. According to eq. 2.27, there is a factor of approximately 15 between the leakage currents at room

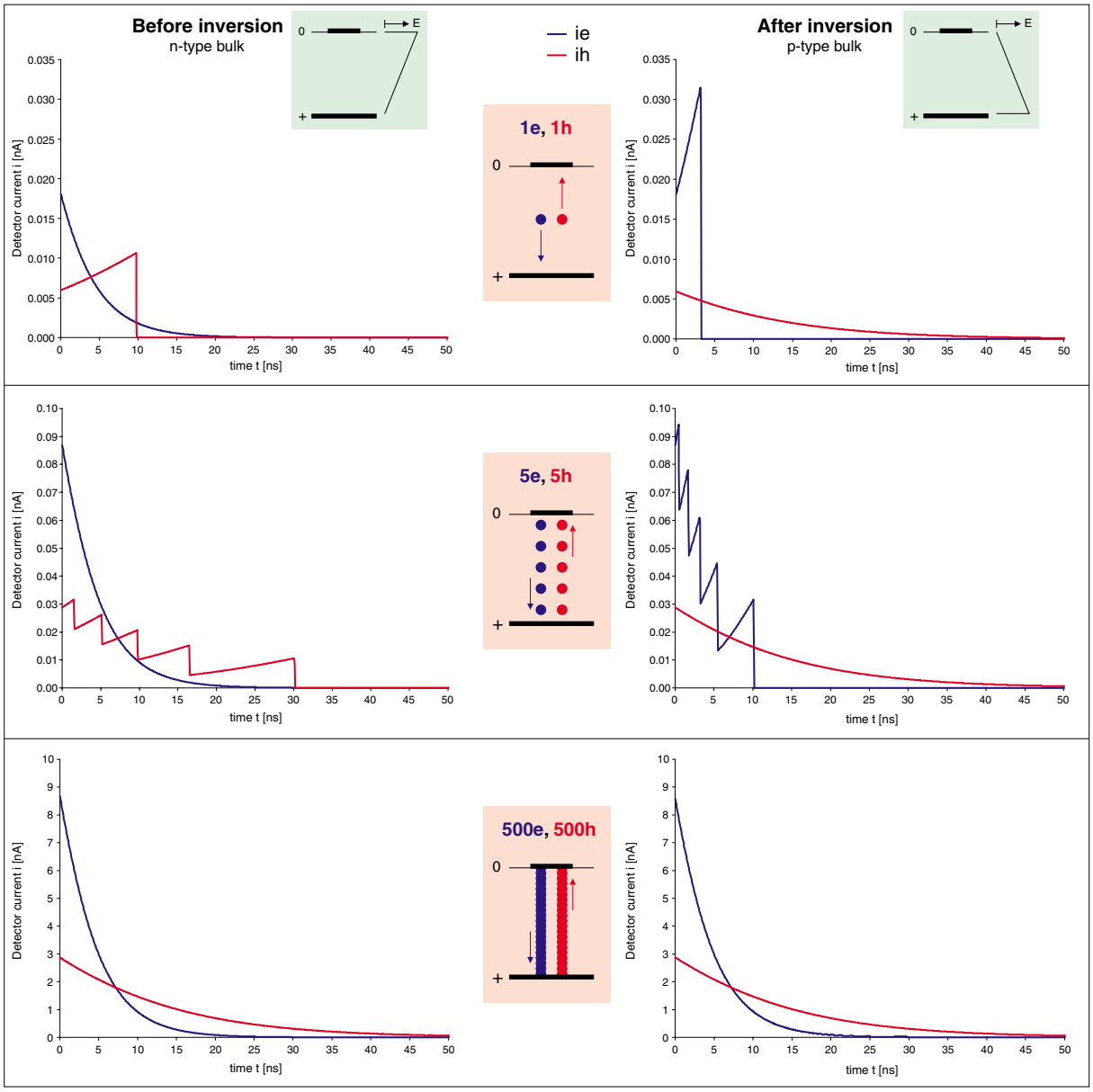



Figure 2.14: Particle induced current waveforms before and after inversion at the depletion voltage. The top plot shows the normalized currents of 2 single charges, which are placed in the center, moving across the bulk to the electrodes. The center plot shows the same for 5 electrons and 5 holes distributed equally along the x axis. In the bottom plot, the same is drawn for a large number of charges, as it happens in a real detector. Gradually the current curves before and after inversion merge.

temperature and at $-10^\circ$ C. Thus, also the proportional factor $\alpha$ as given in eq. 2.26 shows the same temperature dependence. At room temperature, values between 4 and $10 \cdot 10^{-17}$ A/cm are stated for the current related damage rate, depending on the measurement method.

After irradiation, the increased current is still changing. There is a beneficial short-term effect called "annealing" with a time constant of a few days at room temperature. Unfortunately, it is followed by a deterioration effect called "reverse annealing" in the long run (about one year at room temperature). Both effects are strongly temperature dependent. At room temperature, the annealing first causes the leakage current to decrease, while later it rises due to reverse annealing process until it finally saturates at a value which is significantly above the initial level. At $-10^\circ$ C however, both effects are virtually frozen, so the detector current remains constant. Thus, irradiated detectors in general should be operated and stored at low temperature, while it is favorable to shortly expose them to room temperature (for handling, service, transportation etc.) to take advantage of the beneficial annealing.

### 2.3.3 Charge Collection Efficiency

With irradiation, defects are introduced in the silicon bulk which act as charge traps and recombination centers. This leads to a reduction in the charge collection efficiency. The probability of charge trapping is proportional to the drift time of the carriers. Thus, the charge collection efficiency can be partially restored by applying a higher bias voltage, which results in shorter drift times as discussed in section 2.2, p. 17. While the efficiency curve of non irradiated detectors reaches its plateau at the depletion voltage, irradiated sensors need considerable "overbiasing" beyond the depletion voltage. In practice, the efficiency in that case never fully saturates, while the operational voltage is limited by high voltage breakthrough.

Experimental results showing this effect can be found in section 5.1.5.2, p. 89.

## 2.4 Detector Geometry

The primary goal of silicon detectors is to measure a particle track, i.e., the geometrical position of the points where a particle traverses several layers of silicon detectors. Due to its function, a silicon detector is basically limited to two dimensions. With a simple detector with two large-area electrodes as shown in fig. 2.6, p. 19, no geometrical information can be retrieved. This information can only be obtained with a dedicated geometrical layout of one or both electrodes. The two prinicpal layout schemes are strips and pixels, measuring one and two dimensions, respectively.

### 2.4.1 Strips

On strip detectors, the top electrode (at the pn-junction) forms long, thin lines with a typical spacing ("pitch") between 50 and 250 $\mu$m. In a simple readout system, where the position information is derived from the strip with the highest signal, the root mean square (RMS) spatial resolution with pitch $p$ is given by

$$\mathrm{RMS}_{\mathrm{dr}} = \frac{p}{\sqrt{12}} \quad . \tag{2.28}$$

In practice, analog signals of all channels are read out in most cases. This allows advanced signal processing which can significantly improve the spatial resolution, because the charge

is shared between neighboring strips due to capacitive coupling. One possible method is to calculate the center of gravity of the analog signals for a particle's crossing point. Depending on the signal-to-noise (SNR) figure, the spatial resolution can be improved by a factor of up to ten compared to digital with sophisticated signal processing.

Normally, each strips is connected to a separate amplifier channel. In some detector designs, only every second (or even third) strip is read out, while the remaining "intermediate strips" are terminated with high impedance. As there is capacitive coupling, signals on these intermediate strips are partially transferred to the readout strips. With this method, the number of amplifier channels can be reduced, while the performance is naturally worse than with full readout, but still better than without intermediate strips [23].

The electrical connection between strips and amplifier channels is made with a thin wire (typically 25 $\mu$m diameter), welded onto corresponding pads using an ultra-sonic bonding wedge. If the sensor pitch does not match the readout chip input pad spacing, which is usually the case, an intermediate pitch adapter must be used. Fig. 2.15 shows a row of wire-bonds between a silicon detector, the pitch adapter and the readout chip.

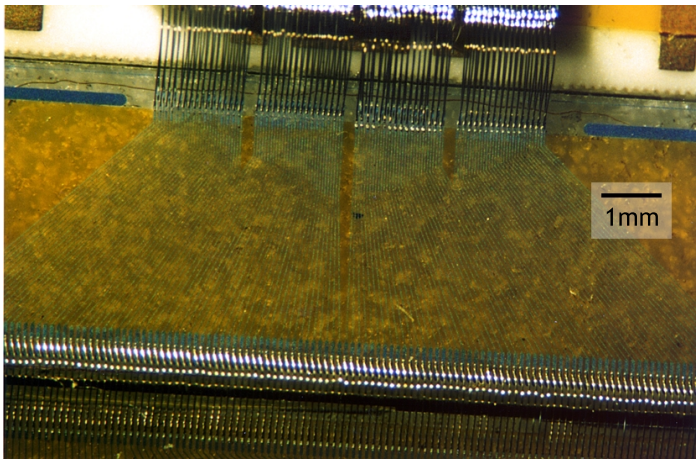



Figure 2.15: Connection between a strip detector (bottom) and the readout chip (top) by micro-bond wires with an intermediate pitch adapter.

The maximum size of a silicon strip detector is determined by the diameter of the silicon single-crystal rod out of which the wafers and later the sensors are cut. Wafers of 4" have been used for more than a decade, while present technology allows to process 6" wafers. Thus, sensors of about $10 \times 10\,\mathrm{cm}^2$ can be produced in a single piece. For larger detectors, two or more strip detectors can be mechanically and electrically chained together in "ladders", thus multiplying the effective strip length. Ladders of 72 cm active length, consisting of twelve sensors, have been successfully built for the silicon target of the WA96 neutrino experiment (NOMAD-STAR) [24] at CERN.

The electrical representation of a strip is a capacitive current source, composed of the backplane capacitance and the interstrip capacitance against neighboring strips. A single strip typically shows a total capacitance of $1\,\mathrm{pF\,cm}^{-1}$. Investigations on prototypes for the CMS silicon tracker [25] revealed that the actual value is independent on the detector thickness in the range of 300 to 500 $\mu$m, because the interstrip capacitance increases while the backplane part decreases and vice versa. However, the total strip capacitance does depend on the ratio of the strip implant

width $w$ and the pitch $p$. The empirical equation

$$C = \left(0.8 + 1.7\frac{w}{p}\right) \text{ pF/cm} \tag{2.29}$$

has been derived from measurements. Fig. 2.16 shows measured values of the total strip capacitance as a function of $w/p$ for three different thicknesses together with fitted lines.

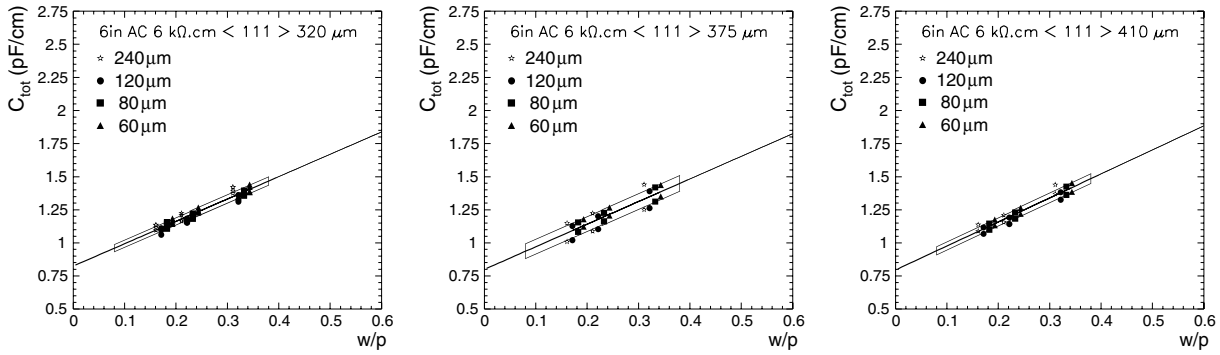



Figure 2.16: Measured total strip capacitance per unit length in silicon detectors of 320, 375 and 410 $\mu$m thickness as a function of implant width over pitch [8].

In practice, the primary restriction of the total strip length is the capacitive load seen by the readout amplifier, which determines the noise figure (see section 2.6.4, p. 36). The strip pitch design has to consider the available budget, the required spatial resolution and the expected particle rate, typically aiming for a single strip hit probability ("occupancy") of a few percent or less.

### 2.4.2 Pixels

When the top electrode is made of tiled rectangular or square pads, the charge is collected on the pad where the particle track crossed the detector. Pad dimensions between 100 $\mu$m and 10 mm have been realized. Small pads (typically below 1 mm) are called pixels.

The spatial resolution improves with smaller pixels. A principal limitation to the pixel size is the readout electronics, since each pixel needs its own amplifier channel. The electrical connection between each sensor pixel and its associated readout channel is not as easily established as with regular strip detectors, where a bond wire is placed between each strip and the corresponding amplifier channel (see section 2.4.1, p. 28). The pixel detector geometry is two-dimensional, but wire-bonding is restricted to one dimension. A possible solution for large pad detectors is to route all pads to a single row of bonding pads on one side of the sensor, as it has been done with the Silicon Detector of the PHOBOS Experiment at RHIC [26, 27]. This method reduces the connection problem to the same procedure as with strip detectors, but it implies some disadvantages: First of all, the capacitive and resistive loads dramatically increase, leading to a higher noise figure, and crosstalk problems can arise. Moreover, the manufacturing of the sensor gets complicated and thus more expensive. Such a routing solution is feasible with a pad size in the millimeter range, but impossible for small pixels as designed for CMS.

The advanced solution is to connect each pixel cell directly to the corresponding readout channel in a sandwich-like compound as shown in fig. 2.17. Each sensor pixel sits directly on top of the corresponding readout chip cell. Small solder bumps (e.g. made of Indium) are applied

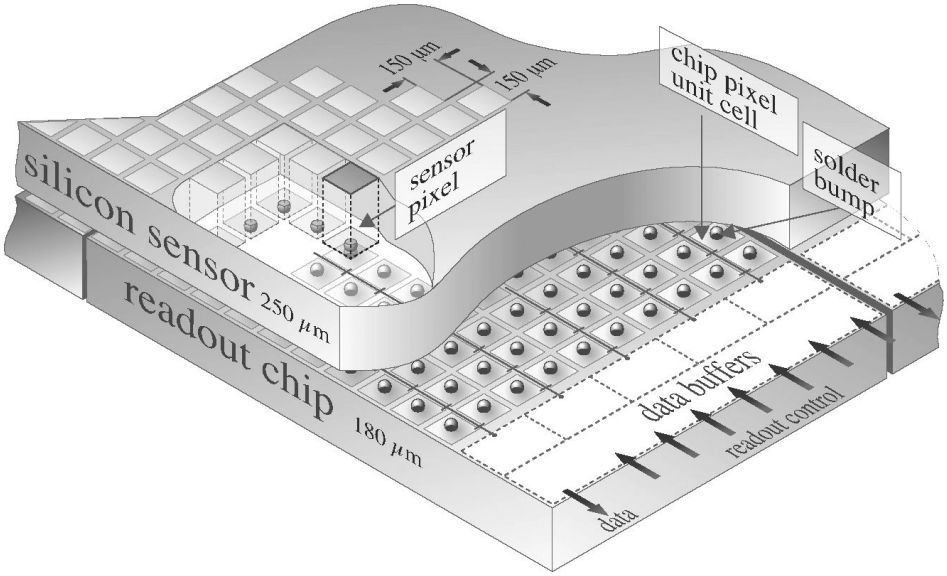



Figure 2.17: A pixel detector, bump-bonded onto the readout chip.

onto one or both sides and treated thermally before the connection is made. Naturally, this procedure is much more complicated than wire-bonding, and there is no possibility to inspect the bump bonds nor to repair broken connections.

Given these difficulties, one might ask why not integrate sensor and electronics onto the same wafer, since both are made of silicon? Unfortunately, the requirements for sensor and electronics grade materials are quite different in terms of bulk doping concentration, purity and operational voltage. Nevertheless, such integrated pixel devices are under development [28], where an epitaxial sensor layer of a few micrometers thickness has been grown onto a pixel chip. Prototypes were successfully operated in a beam test.

## 2.5 Lorentz Shift

Normally, the charge carriers move straight to the electrodes under the influence of the electric field. If a magnetic field perpendicular to the electric field is present, as it is the case in the barrel part of the CMS Tracker, the charges are deflected from their track. A single charge $Q$ moving in electric and magnetic fields $E$ and $B$ with the velocity $v$ will experience the Lorentz[5] force $F$,

$$F = Q\,(E + v \times B) \quad . \tag{2.30}$$

This transverse force due to the magnetic field, also known as known as Hall[6] effect, results in inclined carrier movement relative to the electric field as shown in fig. 2.18. Electrons and holes are subjected to different shifts, since their drift velocities are different. The Hall effect has two consequences: The electrode target area of the charge widens proportional to the detector

[5] Hendrik Antoon Lorentz, *1853 in Arnhem, †1928 in Haarlem (both Netherlands). Dutch phycisist who worked on the relationship between electricity, magnetism and light. In 1902, he was awarded the Nobel Prize for his theory of electromagnetic radiation, which gave rise to Einstein's special theory of relativity.

[6] Edwin Herbert Hall, *1855, †1938. American Physicist who discovered the effect known by his name in 1879.

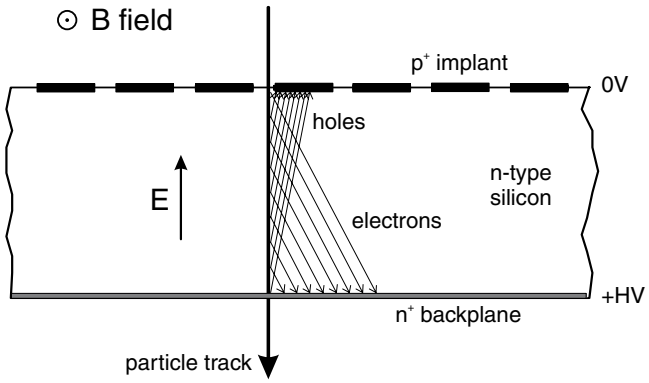



Figure 2.18: Electrons and holes are deflected under the influence of an electric field. This Lorentz shift causes an offset between the particle track and the measured position.

thickness and the target center is offset relative to the particle track. This "Lorentz shift" is usually expressed as an incline angle. With a CMS-like magnetic field of 4 T, Lorentz angles of 31° and 8° have been measured for electrons and holes, respectively, in a silicon detector of 300 $\mu$m thickness [29].

The practical relevance of the Lorentz shift can be minimized by mechanically tilting the detectors such that the target areas on the electrodes of both electrons and holes coincide. With this choice, the equal Lorentz shifts of both carriers can be easily corrected by numerical offset subtraction. In the case of CMS, the corresponding tilt angle is 11.5°.

## 2.6 Readout Electronics

An electronic amplifier is necessary to measure the signals of a semiconductor detector. Among different concepts, an integrating preamplifier with CR-RC shaper is used with most present silicon detectors, so this amplifier type will be described here.

### 2.6.1 Coupling

Each strip or pixel of a silicon sensor must be connected to its own readout channel. This can be done in two different ways. Either, there is a direct connection from the strip or pixel to the amplifier input (DC coupling). This implies that the amplifier must sink a fraction of the detector leakage current that corresponds to the strip or pixel. While this contribution is usually small on pixels because of their limited size, it can be much higher than the signal current especially with irradiated strip detectors. Since the leakage current depends on the applied bias voltage and the radiation damage, it is difficult to build an amplifier which can handle such a wide range of input current. The solution is to bypass the DC leakage current over a resistor and pick up only the AC part over a capacitor (AC coupling). Obviously, this is the preferred technique for present silicon detectors.

With silicon strip detectors, resistors and coupling capacitors are usually integrated into the sensor. The bias resistor is either implemented as a field oxide field effect transistor (FOXFET) or, more common, a polysilicon meander structure, which is less vulnerable to radiation damage. The capacitor is built by a metal layer over silicon oxide on top of the strip implant. The bias voltage, which is applied to the backplane, is usually decoupled with an RC filter. Fig. 2.19

shows the connection schemes for a single channel of a silicon detector with both DC and AC coupling methods.

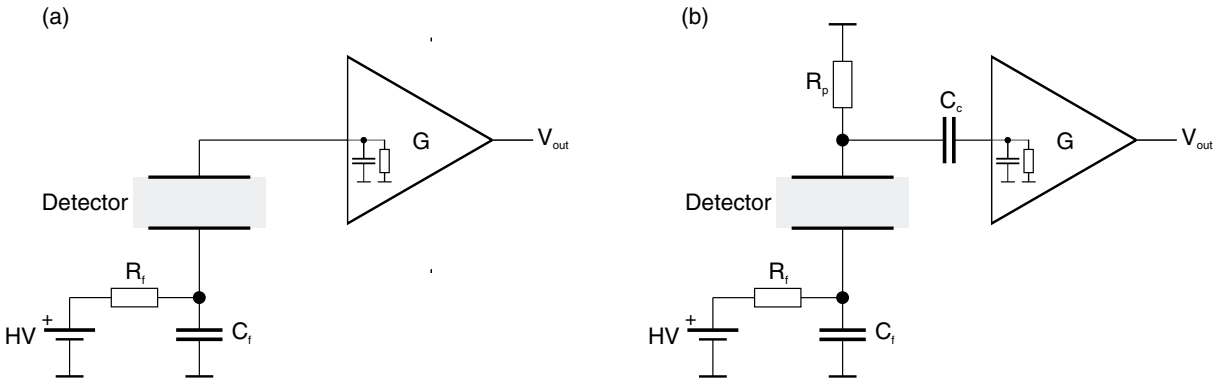



Figure 2.19: Two methods of silicon detector instrumentation: DC coupling (a) and AC coupling (b). In both cases, the backplane bias voltage is filtered by an RC network.

### 2.6.2 Amplifier

While it is possible to build a discrete amplifier for a single or few channels, the huge number of readout channels in high energy physics experiments demands high integration. Present front-end chips usually include 128 separate amplifier channels together with analog bias generators, sample/hold circuits, the associated control logic and a multiplexing output stage. In some cases, a pipeline storage or a digitization circuit are included as well. All of these functions are built into an integrated circuit (IC) with a die size of less than $1\,\mathrm{cm}^2$.

Since a semiconductor detector produces a current signal, the amplifier must have a low-resistance current input. The shape of the current pulse depends on the bias voltage (see section 2.2, p. 17). There are specialized fast low-noise amplifiers which can visualize the current waveform [30], but usually it is more convenient to measure the integrated current, which corresponds to the collected charge. Thus, the first stage of the amplifier is an integrator. As the MIP charge is only 22500 electrons, special attention must be paid to noise minimization, which is done by a special filter ("shaper") in the second stage of the amplifier.

The CR-RC shaping method employs a semi-Gaussian filter which allows easy implementation. Fig. 2.20 shows the principal schematics of an integrating preamplifier together with a CR-RC shaper. With equal resistors, capacitors and thus time constants $T_p = R_i C_i$, the transfer function of such an amplifier in the Laplace domain is given by

$$\frac{V_{\mathrm{out}}}{I_{\mathrm{in}}} = \frac{A\,T_p}{(1 + s\,T_p)^2} \tag{2.31}$$

with the factor $A$ determined by the preamplifier. The practical implementation of this circuitry often includes transconductance amplifiers [31], resulting in a more complicated transfer function. Nevertheless, eq. 2.31 gives a good approximation for that case.

Since the input current pulse is always much shorter than the shaping time constant, it can be approximated by a Dirac-$\delta$ pulse weighted with the collected charge $Q_c$. The amplifier response to such an input is

$$v_{\mathrm{out}} = A\,Q_c\,\frac{t}{T_p}\,e^{-\frac{t}{T_p}} \tag{2.32}$$

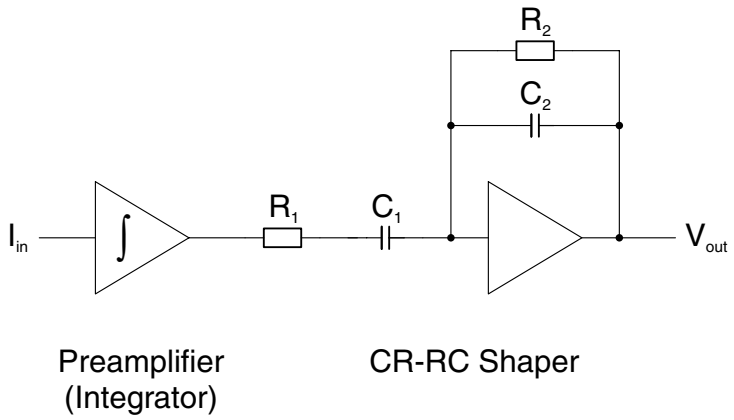



Figure 2.20: The most widely used amplifier principle for silicon detectors: An integrating preamplifier followed by a CR-RC shaper.

in the time domain. Since the maximum output voltage is reached at $T_p$, the time constant is also known as "peaking time".

The simulation discussed in section 2.2, p. 17, has been used to feed an integrating preamplifier with CR-RC shaper with the calculated detector currents and compare the output to the one obtained with an idealized Dirac-$\delta$ input pulse (eq. 2.32). A shaping time of 50 ns, which is also used in the APV amplifier for CMS, was chosen. The simulated amplifier output waveforms with silicon detectors of 300, 400 and 500 $\mu$m thickness are compared to a Dirac-$\delta$ input pulse in fig. 2.21.

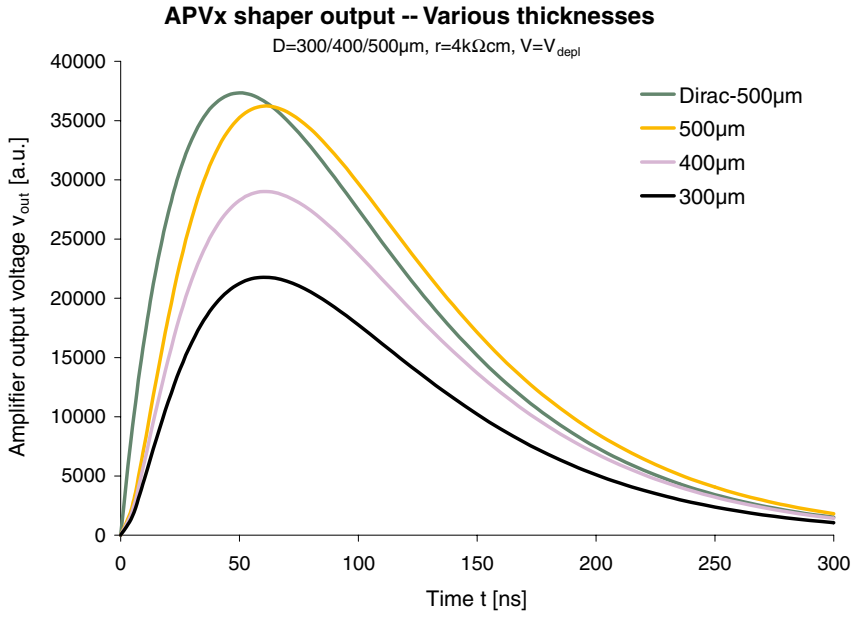



Figure 2.21: APV shaper ($T_p = 50$ ns) output voltage with MIP signals coming from 300, 400 and 500 $\mu$m thick detectors and an ideal Dirac-$\delta$ pulse.

In practice, the preamplifier has a resistor feedback in addition to the integrating capacitor so its output smoothly returns to zero. Thus, drift and saturation are avoided without disturbing

the principal function. However, the time constant of feedback capacitor and resistor must be small enough to avoid pile-up effects with frequent signals.

The preamplifier input, as seen from the detector, is capacitive when neglecting the feedback resistor. Its value is given by the feedback capacitor (typically around 1 pF) multiplied by the open-loop gain (typically 1000), leading to a typical input capacitance of 1 nF. The detector signal current is divided between the strip (or pixel) capacitance and the amplifier input capacitance, so their ratio should be as high as possible towards the amplifier. Taking the above values with a typical strip detector (20 pF), the charge loss is 2% and thus negligible.

### 2.6.3 Deconvolution

Since future high energy colliders are designed for very frequent collisions, the response time of the amplifiers must be fast enough to distinguish particles coming from different bunch crossings. For charge-sensitive amplifiers this implies that the peaking time should be in the order of the bunch crossing period, which is challenging in terms of noise performance. An alternative solution has been developed which works with a larger peaking time. The principal target of the deconvolution method [32, 33] is to restore the original detector current pulse by processing the shaper output signal with a special digital filter.

The shaper output is sampled with the bunch crossing clock frequency and stored in a pipeline. Three consecutive values are added with individual weights to numerically compensate the shaping process. With the sampled shaper output values $p_i$ and the weights $w_i$, the deconvoluted output $d_k$ becomes

$$d_k = w_3\, p_{k-2} + w_2\, p_{k-1} + w_1\, p_k \quad . \tag{2.33}$$

It has been shown that this procedure is exact for an integrating preamplifier followed by a CR-RC shaper using the weights

$$\begin{aligned} w_1 &= A\,\frac{e^{x-1}}{x} \quad , \\ w_2 &= A\,\frac{-2e^{-1}}{x} \quad \text{and} \\ w_3 &= A\,\frac{e^{-x-1}}{x} \end{aligned} \tag{2.34}$$

with the ratio between sampling time and peaking time $x = T/T_p$ and a normalization factor $A$.

The APV chip (see section 4.1, p. 51) of the CMS Silicon Strip Tracker has a peaking time $T_p = 50$ ns and is clocked with the bunch crossing period of $T = 25$ ns. It includes an analog pipeline and an analog pulse shape processor (APSP), which performs the deconvolution using switched capacitors.

The deconvolution method has been included in the silicon detector simulation discussed in section 2.2, p. 17. Fig. 2.22 shows the APV shaper output ("peak mode") and the processed signal ("deconvolution mode"). Although the real output consists of sampled values in steps of the bunch crossing time, continuous waveforms have been calculated for easier comparison.

In fact, the deconvoluted output, when properly timed with respect to the sampling points, is approximately zero except for one sample. Two particles, producing a signals in consecutive bunch crossings, cannot be recognized in the shaper output, but easily after deconvolution. Such a clear separation could not be obtained by simply shaping with a shorter peaking time of

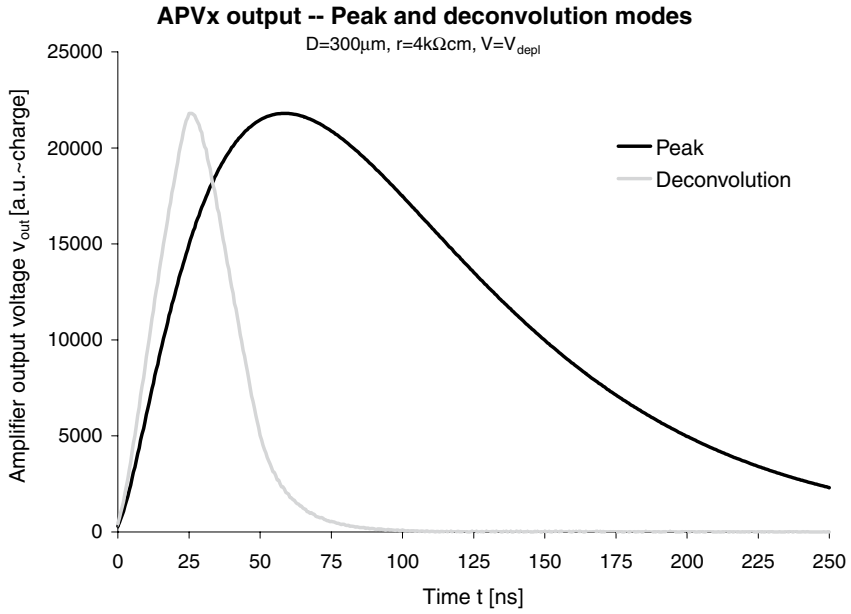



Figure 2.22: APV output in peak and deconvolution modes. In reality, the output is sampled in steps of $T = 25\,\text{ns}$ in both cases, but continuous curves have been calculated for better visualization.

$T_p = 25\,\text{ns}$, because the long tail would result in a few non-zero samples after the peak. Thus, the deconvolution method is a powerful tool for unambiguous bunch crossing separation. This advantage has to be paid off by an increased noise figure, as discussed in the following section.

### 2.6.4 Noise

The noise in a silicon detector system plays an essential role, since the signals are very low. Especially with strip detectors, it is important to know each contribution to optimize the design. This is easier for pixel detectors, since their active area is very small and there is virtually no readout line impedance, which reduces many noise components down to negligible values compared to strip detectors.

The electronic noise in silicon detector systems is given in terms of equivalent noise charge (ENC) referred to the input. The main noise source is the input transistor in the amplifier, with a noise figure depending on geometry and electrical parameters [24, 31, 34, 35]. Noise contributions of further electronic stages are usually neglected. Due to its integrating nature, the load capacitance plays an important role for the amplifier noise. In a simple approach, the amplifier noise can be described by the sum of a constant value (parallel noise) and a part which scales with the load capacitance $C$ (series noise),

$$\text{ENC}_\text{C} = \text{ENC}_{\text{C,p}} + \text{ENC}_{\text{C,s}}\, C \quad . \tag{2.35}$$

With the capacitive load which is typical for a strip detector, the amplifier noise can be as small as 250 e with a peaking time of a few microseconds. When faster shaping is required, the noise increases. The CMS front-end amplifier APV25 with a peaking time of $T_p = 50\,\text{ns}$ has a noise figure of about 970 e with a typical capacitive load.

Apart from the amplifier, there are other noise sources in the system. Fig. 2.23 shows noise related components in a typical AC coupled strip detector configuration with a polysilicon bias

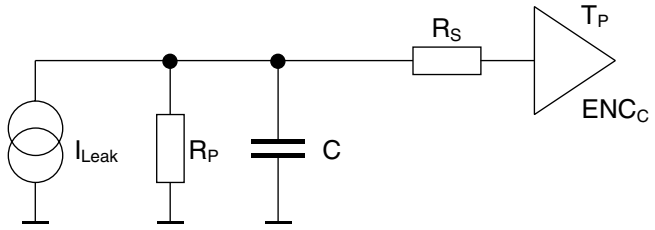



Figure 2.23: Noise sources in a silicon strip detector.

resistor. The AC coupling capacitor can be neglected in these considerations. The current source $I_{\mathrm{Leak}}$ is the fraction of the detector leakage current which is seen by one strip, $R_P$ is the polysilicon resistor, $C$ is the detector strip capacitance and $R_S$ is the line resistance of the strip. In reality, the line resistance and the strip capacitance are distributed along the strip as in a transmission line, so the effective impedance differs from the concentrated values. Nevertheless, its influence is limited, so we will use the concentrated values as an approximation.

Parallel noise sources are the constant part of the amplifier $\mathrm{ENC_{C,p}}$, leakage current fluctuations $\mathrm{ENC_{ILeak}}$ and the polysilicon resistor noise $\mathrm{ENC_{RP}}$. The capacitive fraction of the amplifier noise $\mathrm{ENC_{C,s}}$ and the readout line resistor noise $\mathrm{ENC_{RS}}$ are series noise sources. As expected, the peaking time $T_p$ plays an key role in the noise functions. Numerical noise equations, in which the physical constants are already expressed by numbers, can be written as

$$\mathrm{ENC_{Ileak}} = 106\sqrt{I_{\mathrm{Leak}}\,T_p} \quad , \tag{2.36}$$

$$\mathrm{ENC_{RP}} = 758\sqrt{\frac{T_p}{R_P}} \quad \text{and} \tag{2.37}$$

$$\mathrm{ENC_{RS}} = 0.395\,C\sqrt{\frac{R_S}{T_p}} \tag{2.38}$$

with ENC [e], $I_{\mathrm{Leak}}$ [nA], $T_p$ [$\mu$s], $R_P$ [M$\Omega$], $R_S$ [$\Omega$] and $C$ [pF]. Parallel noise contributions rise with increasing peaking time, while series noise behaves opposite. The total noise figure is the square sum of the individual contributions, since the individual sources are uncorrelated,

$$\mathrm{ENC^2} = \sum \mathrm{ENC_i^2} \quad . \tag{2.39}$$

The deconvolution method (see section 2.6.3, p. 35) compromises the noise. Both intrinsic amplifier noise components increase due to the signal processing and the external series noise is amplified, while the parallel noise is reduced. It has been shown [32, 33] that the ratio between peak and deconvolution mode noise can be expressed for parallel and series terms as

$$\frac{\mathrm{ENC_{p,d}}}{\mathrm{ENC_p}} = \frac{e^{-2}}{x^2}\left(e^{2x} - 4x - e^{-2x}\right) \quad \text{and} \tag{2.40}$$

$$\frac{\mathrm{ENC_{s,d}}}{\mathrm{ENC_s}} = \frac{e^{-2}}{x^2}\left(e^{2x} + 4x - e^{-2x}\right) \quad , \tag{2.41}$$

where $x = T/T_p$ is the ratio between sampling time and peaking time.

To get a feeling for the magnitude of individual noise components, these figures will be calculated and compared for the DELPHI Very Forward Tracker (VFT) [23] and an average

CMS silicon detector. The VFT uses the MX6 readout chip, while the CMS strip detectors will be instrumented with the APV25 described in section 4.1, p. 51. The APV25 noise will be shown for both peak and deconvolution modes.

| | **DELPHI VFT** | **CMS** |
|---|---|---|
| Amplifier | MX6 | APV25 |
| $I_{\text{Leak}}$ [nA] | 0.3 | 100 |
| $R_P$ [MΩ] | 36 | 1.5 |
| $C$ [pF] | 9 | 18 |
| $R_S$ [Ω] | 25 | 50 |
| $T_p$ [μs] | 1.8 | 0.05 |
| $\text{ENC}_\text{C}$ [e] | $325 + 23\,\text{pF}^{-1}$ | $250 + 36\,\text{pF}^{-1}$ (peak)<br>$400 + 60\,\text{pF}^{-1}$ (deconvolution) |

Table 2.1: Noise related numbers of the DELPHI Very Forward Tracker (VFT) and an average CMS strip detector. The VFT uses FOXFET bias resistors with a dynamic resistance at operating conditions as shown and the leakage current of the CMS detector corresponds to a moderately irradiated state.

| | **DELPHI VFT** | **CMS** | |
|---|---|---|---|
| | | peak | deconvolution |
| $\text{ENC}_\text{C}$ [e] | 532 | 898 | 1480 |
| $\text{ENC}_\text{Ileak}$ [e] | 78 | 237 | 103 |
| $\text{ENC}_\text{RP}$ [e] | 169 | 138 | 60 |
| $\text{ENC}_\text{RS}$ [e] | 13 | 225 | 345 |
| ENC [e] | 564 | 966 | 1524 |
| $\text{SNR}_\text{MIP}$ | 39.9 | 23.3 | 14.8 |

Table 2.2: Noise numbers resulting from the typical values given in tab. 2.1. The total noise in the second last row is the square sum of the above contributions, and the signal-to-noise ratio with a MIP charge of 22500 e is shown below.

Tab. 2.1 gives an overview of typical detector and readout parameters, while the resulting noise contributions are shown in tab. 2.2. The dominant noise source of both detector systems is the amplifier chip, whose contribution principally depends on the peaking time. It is obvious that the signal-to-noise-ratio (SNR) was not an important issue in DELPHI, while it is a crucial figure for CMS especially with the deconvolution method, which will be the default mode of operation.

The noise figures given here include the detector together with the input transistor of the front-end amplifier. In reality, other components in the read-out chain beyond this point also contribute to the total observed noise. Line drivers and receivers, the transmission line and the digitization typically add a few hundred electrons of noise. However, since this contribution is uncorrelated as well, the total square sum is still dominated by the front-end noise.

### 2.6.5 Radiation Damage

Unlike silicon detectors, where the whole volume contributes to the charge collection, only the surface is active in integrated circuits. All the active and passive components are built into a thin layer (approximately 1 μm), while the silicon bulk is inactive.

There are several effects of radiation to integrated circuits. Most of them are related to ionizing particles similar to silicon detectors. Tab. 2.3 summarizes the effects which must be considered in future collider experiments such as CMS.

| Effect | Scope | Persistent |
|---|---|---|
| Single Event Upset (SEU) | digital<br>analog | no<br>no |
| Single Event Latchup (SEL)<br>Single Event Gate Rupture (SEGR) | digital | yes |
| Oxide Charging | analog | yes |

Table 2.3: Important effects of radiation on integrated circuits in the environment of future high energy collider experiments.

A digital SEU (single event upset) occurs when enough charge is deposited close to sensitive areas of a flip-flop cell such that the cell state flips. This can be the result of the high local ionization of a recoil atom produced by a nuclear interaction. Such a flipped memory cell disturbs the state machine of the circuit or register settings stored in such flip-flop cells. An SEU is non-destructive and the aftermath can be cleaned by resetting the circuit and possibly reloading the memory registers. It is possible to reduce the impact of SEUs by introduction of "triple-voting". This design feature foresees three flip-flop cells in parallel where the state is determined by a majority vote. Thus, a single cell can flip without disturbing the circuit and a single event upset can be reported or even self-repaired.

In analog circuits, an SEU can induce transients which might be misinterpreted as signals. For example, the analog pipeline in the APV front-end amplifier stores the sampled output of the shaper stage in capacitors. Naturally, these elements are susceptive to SEUs, resulting in fake signals.

When the localized charge deposition is strong enough to produce a conductive channel between power levels (e.g. in a CMOS inverter) a high current state is produced which is likely to exceed the chip specifications. Such a SEL (single event latchup) or SEGR (single event gate rupture) can destroy the circuit by overheating. A fast (electronic) fuse can avoid such damage if power is taken away immediately.

Radiation also affects the oxide between gate and channel of a CMOS transistors, which leads to changes in channel noise and transconductance. With proper design, these changes are not critical, especially when the bias currents and voltages of amplifiers can be adjusted. In contrast to silicon detectors, the doping concentration levels of integrated circuits are higher by orders of magnitude, such that the radiation induced change is negligible.

There are specialized radiation hard manufacturing processes which were originally developed for military and space applications. An example of such a process, in which prototypes of the CMS tracker electronics were built, is the DMILL technology by Temic [36]. Fortunately, commercial submicron processes which are very popular for integrated circuits today, are intrinsically radiation tolerant due to their small structures. Together with special radiation tolerant design rules such as guard rings around vulnerable cells or triple-voting, this technology offers an inexpensive alternative to specialized radiation hard processes. The CMS Silicon Strip Tracker electronics will be entirely manufactured in the standard IBM 0.25 $\mu$m deep submicron CMOS process [37].

# Chapter 3

# CMS Tracker System

The CMS Tracker is completely made of silicon detectors, which are the best choice for tracking purposes in the LHC environment. In present and past experiments, large-volume gas detectors were a (cheaper) alternative to silicon, but they have a slower response time, so that the LHC timing requirements do not allow their usage.

The tracker consists of a central (barrel) part with three pixel and ten strip layers and the disk and endcap sections with two pixel and twelve strip layers [38]. A cross-section of one quadrant is shown in fig. 3.1. The pixel layers in barrel and endcap parts are shown in purple, while the strip layers are drawn in red (single-sided detector modules) and blue (double-sided detector module). The double-sided modules are made of two single-sided detectors mounted back to back with a strip inclination of 5.7° against each other. Thus, these "stereo" modules deliver two-dimensional hit positions.

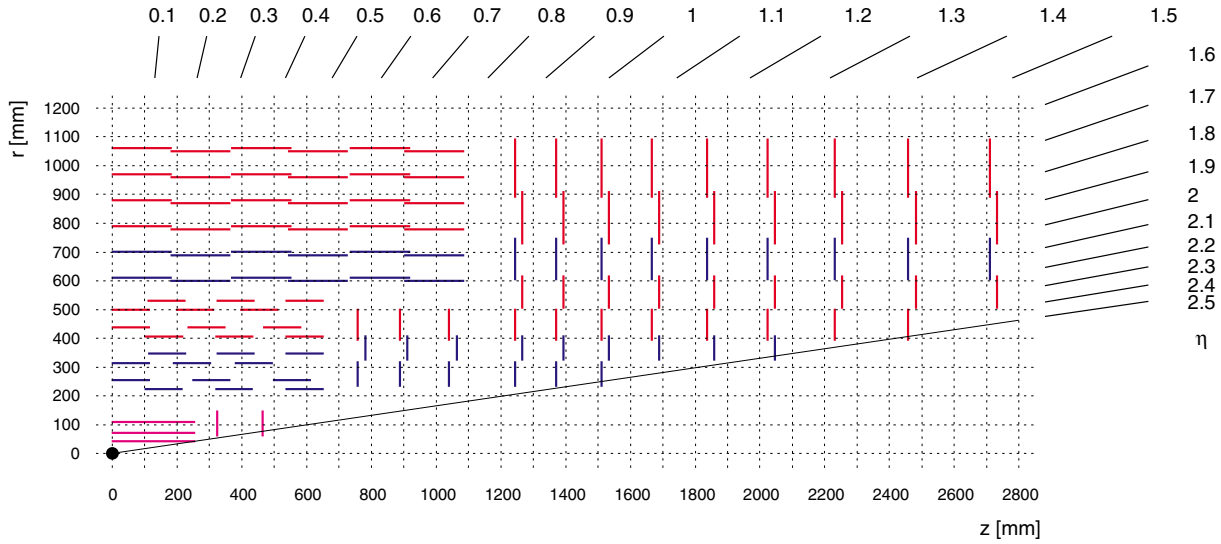



Figure 3.1: One quarter of the CMS Tracker layout. Pixel detector layers are shown in purple, while strip detectors are in red (single-sided) and blue (double-sided). The origin denotes the collision point and the numbers on top and right give the angle in units of pseudorapidity $\eta$, which is a function of radius $r$ and the distance $z$ along the beam axis (eq. 1.3, p. 11).

The number of detector layers is a tradeoff between tracking efficiency, material budget and cost. On one hand, the number of hits increase with the number of layers penetrated, which

makes the track reconstruction easier. On the other hand, the amount of material within the tracker should be kept as low as possible, because multiple scattering, which spoils the tracks, is proportional to the amount of material traversed by the particles. An even tougher constraint is the cost of the tracker, which reduces the number of layers to an affordable design. Simulations on various tracker configurations finally led to the geometry shown in fig. 3.1.

In an average event, about 750 charged particles arise from each bunch crossing, which produce a few thousand hits in the tracker. Fig. 3.2 shows a simulated CMS event where a Higgs boson with a mass of 150 GeV decays into four muons in two projections. Physicists claim that they can extract and identify single particles out of the detector data. In fact this seems possible when keeping in mind that the tracker granularity is very small and thus the occupancy is still reasonably low, while fig. 3.2 only shows two-dimensional projections. Most of the particles are of low momentum (below 1 GeV/c) and thus of no interest with respect to the physics goals. Due to the high magnetic field of 4 T in the tracker, their tracks are bent with a small radius (according to eq. 1.4) such that many of them will not be able to exit the tracker at all. The helix traces of these particles are displayed as circles or sine curves in the shown projections.

The simplest approach to track reconstruction from a set of hit points is to start with a pixel hit in the innermost layer and project a cone onto the next layer in radial direction. If no hit can be found there, the starting point was either noise or a particle of very low energy which get stuck or was deflected by multiple scattering, so the original hit can be discarded. Otherwise, the procedure can be repeated until finally the full track through all planes is found. Of course, the procedure is much more complicated in reality: Dead or inefficient regions have to be taken into account (e.g., by skipping a layer) and the magnetic field bends the tracks depending on the particle momentum. Since there is a lot of low-momentum background in the innermost part of the tracker, a more advanced concept starts its track search from the outside. With this approach, a preselection of interesting tracks is provided by the first-level trigger, which is obtained from calorimeter and muon detector data.

The operating temperature of the CMS tracker will be $-10^\circ$ C. This is required by the silicon sensors, which suffer from radiation damage. Defects are "frozen" so they can not gradually decrease the detector quality, as discussed in section 2.3, p. 23.

## 3.1 Pixel Detector

The high resolution pixel detector [39] is the innermost part of the CMS Tracker. Since the particle density is very high, a small-scale pixel geometry is required for unambiguous hit recognition and precise vertex reconstruction. Short-lived particles arise from the primary vertex, which can decay after having travelled only a few hundred micrometers. The pixel detector must distinguish such secondary vertices from the original collision point.

The barrel part consists of three pixel layers at radii of 4.3, 7.2 and 11.0 cm. The innermost layer will only be present in the initial low-luminosity phase of LHC, since radiation damage will destroy this layer at a later stage. Fig. 3.3 shows the layout of the pixel detector in the 2-layer high-luminosity configuration.

The CMS pixel detector includes a total of about 45 million pixels with a cell size of $150 \times 150\,\mu\mathrm{m}^2$. A grid of $52 \times 53$ pixels is read out by a custom ASIC [40, 41] called DM_PSIxx (where xx is the version number). Currently, the chip is manufactured in radiation hard DMILL technology by Temic [36], but the transition to the deep submicron CMOS process is being

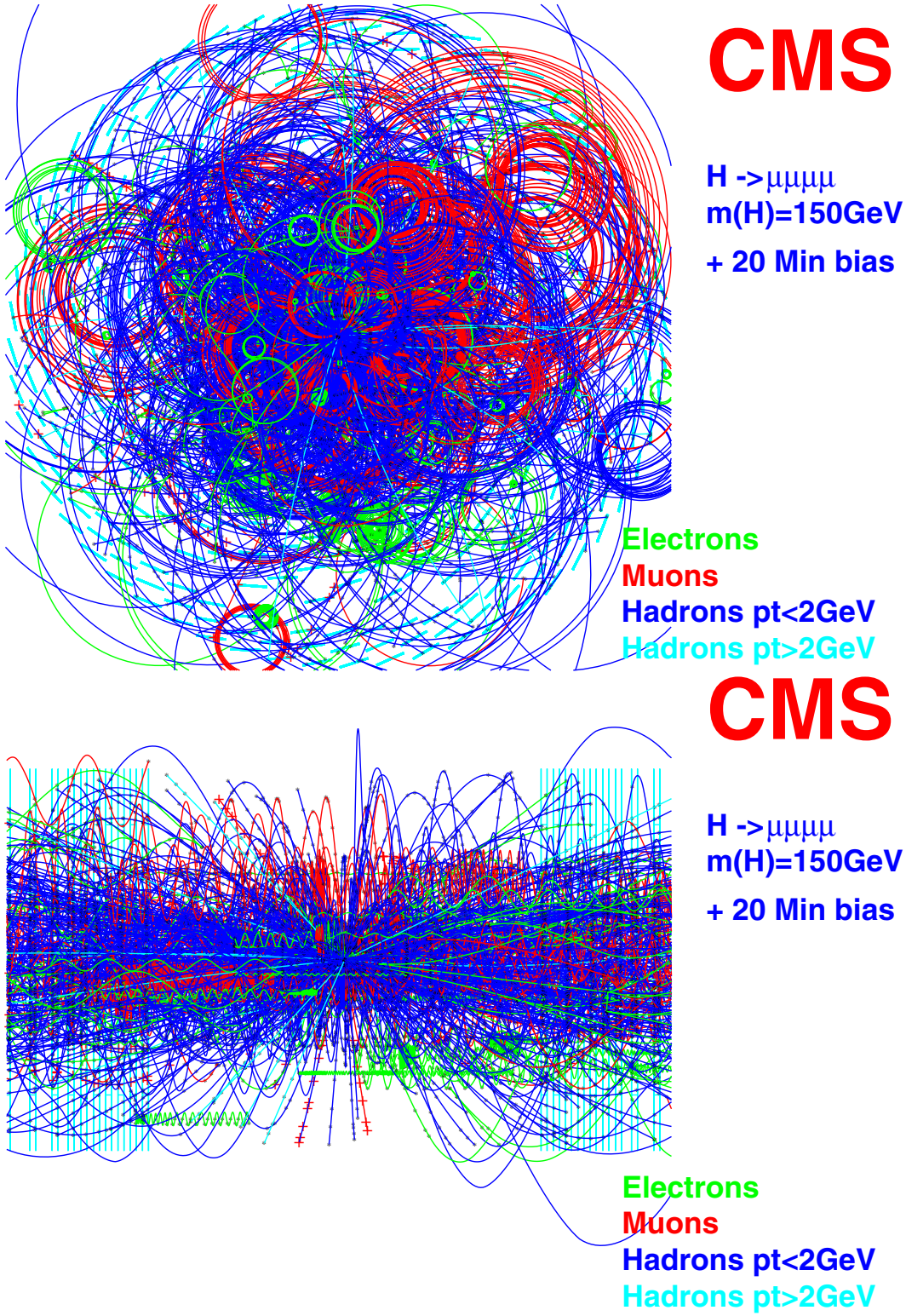



Figure 3.2: Simulated CMS event in $r\phi$ (top) and $rz$ (bottom) projections. A Higgs with a mass of 150 GeV decays into four muons. It is difficult to spot the muons in the tracker, but they are clearly identified in the muon detector, which is the outermost subsystem (see section 1.3, p. 11).

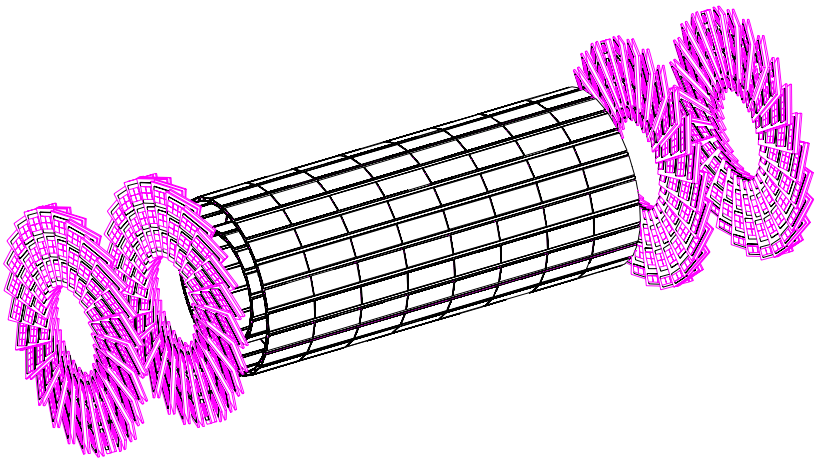


Figure 3.3: The high-luminosity configuration of the CMS pixel detector.

prepared. The readout chip incorporates a separate amplifier for each pixel cell together with an adjustable threshold discrimination, channel multiplexing and the associated digital logic.

Several pixel chips together with one or more sensor tiles and a common control logic make up a module, which is the basic building block of the pixel detector. Fig. 3.4 shows a barrel pixel module on the left. The three pixel layers are composed of 160, 256 and 384 such modules, with an average of 15 chips per module.

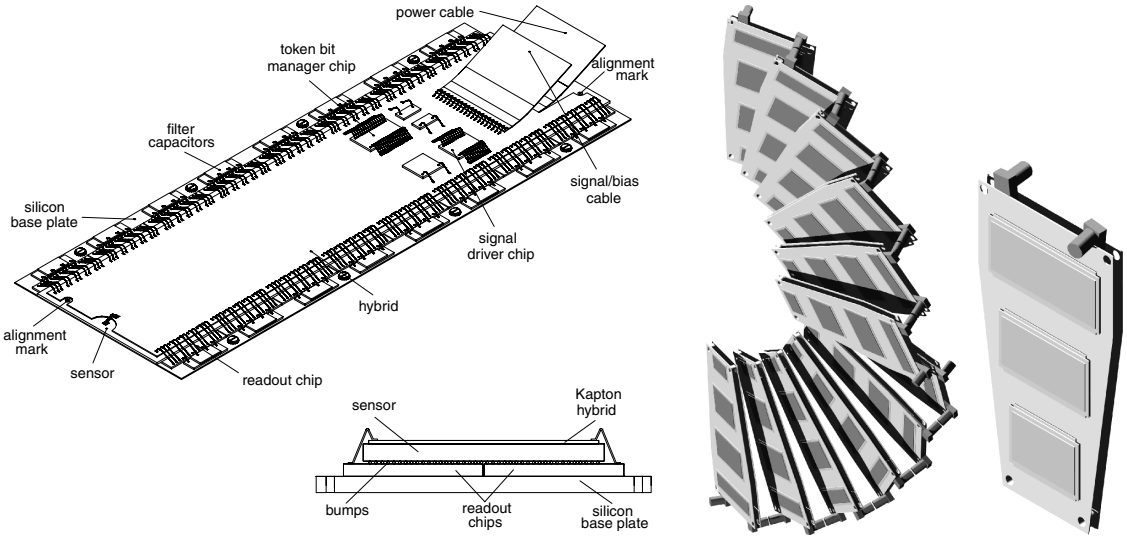



Figure 3.4: Left: A barrel pixel module. Right: The endcap pixel blade layout.

Each disk is divided into 24 blades. The right side of fig. 3.4 shows one half of a disk together with a single blade. Each blade holds four sensors on one side and three on the opposite side, which slightly overlap to ensure full coverage.

The schematics of a single pixel unit cell (PUC) is shown on the left part of fig. 3.5, including an integrating preamplifier with CR-RC shaper stage in the analog block. A calibration pulse can be injected over a capacitor to test the electronics, whereas the usual input is from the pixel sensor cell. The shaper output is then sent into the comparator stage, which has a global

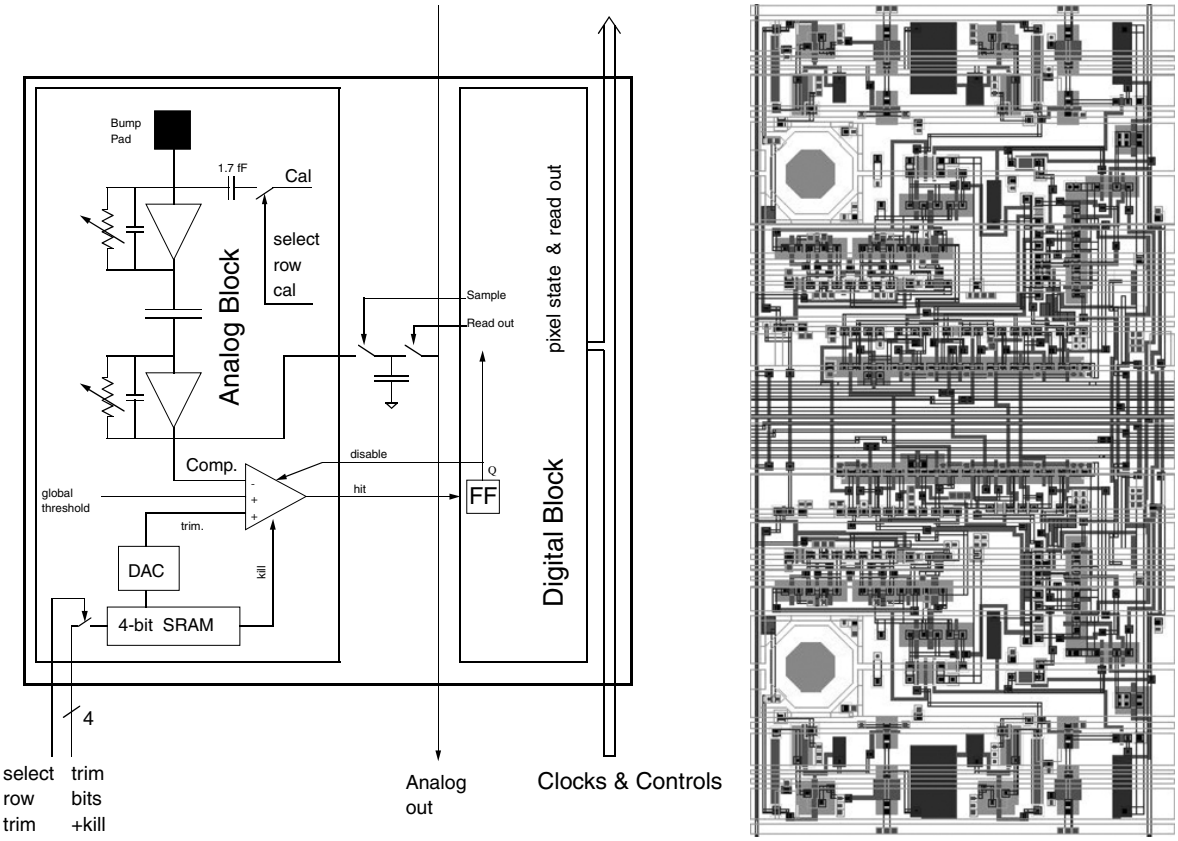



Figure 3.5: Left: Schematics of a pixel unit cell (PUC). Right: Layout of two adjacent PUCs on the DM_PSI32 prototype die.

threshold. To deal with channel-to-channel variations, the threshold of each individual cell can be fine-tuned with a 3-bit value which is transformed into analog with the cell DAC. A fourth register is used to turn off the discriminator completely which allows to switch off noisy pixels. When a PUC reports a hit, the analog shaper output is read out using a sample/hold circuit and stored in a buffer together with position information and a timestamp. On the arrival of a first-level trigger, the corresponding buffer cells are coded and multiplexed onto the output line. The die layout of two adjacent PUCs of the DM_PSI32 prototype chip is shown on the right side of fig. 3.5. The large dots are intended for the bump-bonding connections to the sensor.

## 3.2 Strip Detector

The Silicon Strip Tracker (SST) of the CMS experiment covers an area of 206 $m^2$, which makes it the largest silicon detector under construction. The sensors are arranged in a total number of about 20000 modules, which consist of one or two strip detectors in series together with the associated readout electronics. Depending on the position within CMS, the geometry of the sensors and the number of readout strips varies: In the barrel region, the sensors are rectangular, while the endcap sensors are of trapezoidal shape to fit together in discs (fig. 3.6).

The barrel modules will be placed on the surface of cylindrical support structures as shown on the left side of fig. 3.7. To allow better area coverage, the modules will overlap like roof tiles,

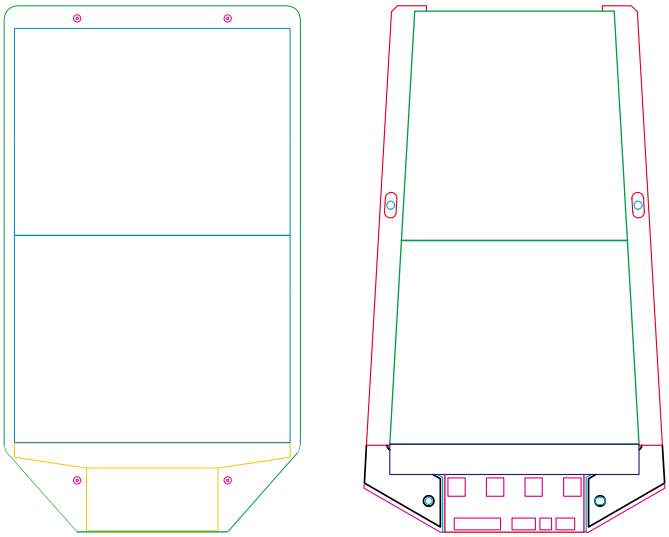


Figure 3.6: Layout of the silicon modules in the barrel (left) and endcap (right) regions.

Figure 3.7: Left: Prototype support structure for the barrel with mounted dummy detector modules. Right: Same for an endcap disk.

which causes a tilt angle of 9 to 12° out of the tangential plane, approximately resulting in an equal Lorentz shift of electrons and holes (see section 2.5, p. 31). In the disks (right part of fig. 3.7) however, there is no Lorentz shift and thus no tilt, since electric and magnetic fields have the same direction.

A carbon fiber frame holds one or two silicon sensors which are connected to the readout hybrid via a pitch adapter. Each module has 512 or 768 strip channels which are read out by four or six chips, respectively. On both ends of the frame, cooling pipes are sinking the heat produced by sensors and electronics.

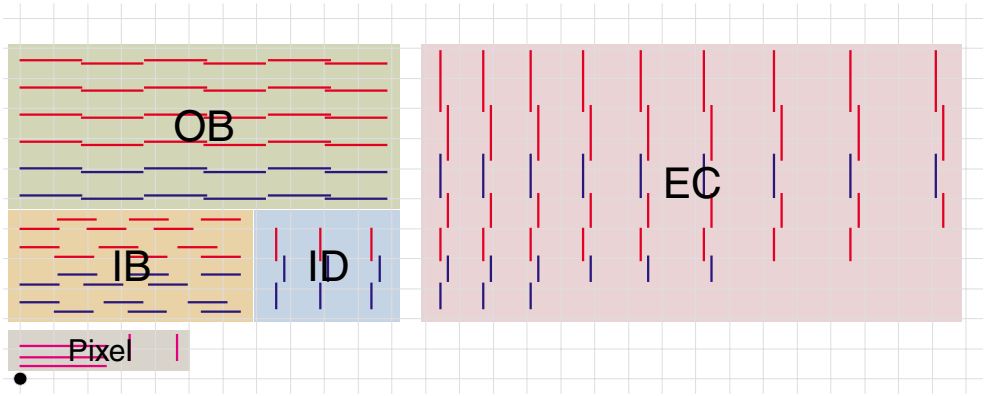



Figure 3.8: Functional groups of the CMS silicon tracker: inner barrel (IB), outer barrel (OB), inner disks (ID) and endcaps (EC).

Fig. 3.8 shows the functional groups of the CMS silicon tracker. The ten strip layers in the barrel are divided into the inner barrel (IB) and the outer barrel (OB), which are numbered in ascending order with the radius. The seven rings of the disk modules are divided into the inner disks (ID) and the endcaps (EC), again numbered with ascending radius.

The properties of the barrel and disk silicon detectors are given in tab. 3.1 and 3.2, respectively.

| **Layer** | **Radius** [mm] | **Type** | **Modules** | **Pitch** [$\mu$m] | **Strips** |
|---|---|---|---|---|---|
| IB 1 | 250 | double-sided | 336 | 80 | 768 |
| IB 2 | 340 | double-sided | 456 | 80 | 768 |
| IB 3 | 430 | single-sided | 552 | 120 | 512 |
| IB 4 | 520 | single-sided | 648 | 120 | 512 |
| OB 5 | 610 | double-sided | 504 | 122/183 | 768/512 |
| OB 6 | 696 | double-sided | 576 | 122/183 | 768/512 |
| OB 7 | 782 | single-sided | 648 | 183 | 512 |
| OB 8 | 868 | single-sided | 720 | 183 | 512 |
| OB 9 | 965 | single-sided | 792 | 122 | 768 |
| OB 10 | 1080 | single-sided | 888 | 122 | 768 |

Table 3.1: Mechanical dimensions and numbers of the CMS silicon barrel detectors. The stated radii from the beam action are average values, since the modules are tilted. Double-sided modules count only once.

The acceptance criteria for the silicon detectors of the CMS tracker have been worked out in great detail [42], where the most important specifications common to all sensors are:

| Layer | Radius [mm] | Type | Modules | Pitch [$\mu$m] | Strips |
|---|---|---|---|---|---|
| ID 1 | 277 | double-sided | 144 | 81 ... 112 | 768 |
| ID 2 | 367 | double-sided | 144 | 113 ... 143 | 768 |
| ID 3 | 447 | single-sided | 240 | 124 ... 158 | 512 |
| EC 1 | 277 | double-sided | 144 | 81 ... 112 | 768 |
| EC 2 | 367 | double-sided | 288 | 113 ... 143 | 768 |
| EC 3 | 447 | single-sided | 640 | 124 ... 158 | 512 |
| EC 4 | 562 | single-sided | 1008 | 113 ... 139 | 512 |
| EC 5 | 677 | double-sided | 720 | 126 ... 156 | 768 |
| EC 6 | 891 | single-sided | 1008 | 163 ... 205 | 512 |
| EC 7 | 991 | single-sided | 1440 | 140 ... 172 | 512 |

Table 3.2: Mechanical dimensions and numbers of the CMS inner disk and endcap detectors. The stated radii are measured in the center of the active area of each layer. Double-sided modules count only once. The pitch varies due to the wedge-shaped sensors.

- $< 100 >$ crystal orientation
- $p^+$ strip implants on n-type bulk silicon
- Breakdown voltage $> 500\,\mathrm{V}$
- Less than 2% noisy strips
- Polysilicon resistor $R_P = 1.5 \pm 0.3\,\mathrm{M\Omega}$
- Ratio of implant width to pitch $w/p = 0.25$

Standard silicon material has been chosen since it can withstand the radiation levels, while oxygen enriched sensors (see section 2.3.1, p. 25) are considered not yet known well enough and thus implicate a certain risk.

| Type | Wafer size | Sensors per module | Sensor Area [mm$^2$] | Thickness [$\mu m$] | Resistivity [k$\Omega$ cm] |
|---|---|---|---|---|---|
| IB | 4" (6") | 2 (1) | $63.4 \times 119.2$ | $320 \pm 20$ | 1.5 ... 3.0 |
| OB | 6" | 2 | $96.4 \times 189.0$ | $500 \pm 20$ | 3.5 ... 6.0 |
| ID1/EC1 | 6" | 1 | $64.1 \ldots 88.1 \times 89.5$ | $320 \pm 20$ | 1.5 ... 3.0 |
| ID2/EC2 | 6" | 1 | $88.2 \ldots 112.4 \times 90.3$ | $320 \pm 20$ | 1.5 ... 3.0 |
| ID3/EC3 | 6" | 1 | $65.0 \ldots 83.2 \times 112.8$ | $320 \pm 20$ | 1.5 ... 3.0 |
| EC4 | 6" | 1 | $59.9 \ldots 73.4 \times 117.4$ | $320 \pm 20$ | 1.5 ... 3.0 |
| EC5 | 6" | 2 | $99.0 \ldots 112.4 \times 84.0$<br>$112.4 \ldots 123.0 \times 66.1$ | $500 \pm 20$ | 3.5 ... 6.0 |
| EC6 | 6" | 2 | $86.1 \ldots 97.5 \times 99.0$<br>$97.5 \ldots 107.6 \times 87.8$ | $500 \pm 20$ | 3.5 ... 6.0 |
| EC7 | 6" | 2 | $74.1 \ldots 82.9 \times 109.8$<br>$82.9 \ldots 90.9 \times 98.8$ | $500 \pm 20$ | 3.5 ... 6.0 |

Table 3.3: Specifications of the silicon barrel and disk sensors. For the trapezoidal sensors, base and top edge lengths are stated together with the height. The three outermost endcap layers consist of two sensors with different geometry (otherwise they could not be chained together).

The sensors used in the various parts differ considerably. Tab. 3.3 gives an overview of the detector specifications. The inner barrel modules will be fabricated either of two chained 4" wafers or of a single 6" wafer resulting in the same total area. Since the inner part is exposed to a higher radiation dose, its sensors are made of low-resistivity material which reach the inversion point at higher fluence (see section 2.3.1, p. 25). The outer modules, which are a replacement of the previous MSGC design, have longer strips, resulting in an increased capacitive load. As pointed out in section 2.6.4, p. 36, this implies a higher noise figure. To restore a reasonable signal-to-noise ratio (SNR), the sensors are thicker, so that the higher energy loss of traversing particles can compensate additional noise. High-resistivity sensors are required since the depletion voltage scales with the square of the thickness and the inverse resistivity. The radiation level in the outer part is sufficiently low so that the material will not get far beyond the inversion point.

In the innermost layer of the CMS strip tracker, the occupancy is approximately 5%, decreasing to 0.2% in the outermost layer. Fig. 3.9 shows that every energetic particle arising from a collision traverses between eight and fourteen detectors in the silicon tracker [43], depending on the pseudorapidity $\eta$. Double-sided layers are counted only once. The reason why the number of radial hits can exceed the number of detector layers is that there is some overlap between adjacent sensors to ensure full coverage, which occasionally results in two hits in the same plane.

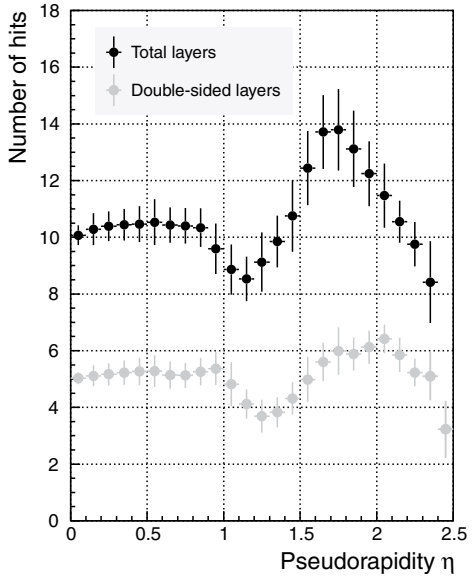



Figure 3.9: The average number of detector planes hit by high energetic particles when travelling through the CMS strip tracker. Double-sided layers count only once.

Several institutes (including the HEPHY) will assemble the CMS silicon strip detector modules using automatic and semi-automatic machinery. The modules will be fabricated with an internal precision of about 5 $\mu$m in the sensor plane and approximately 30 $\mu$m in the coordinate perpendicular to that plane [44]. After a mechanical survey procedure, the absolute position of each strip in space will be known with an accuracy better than 10 $\mu$m. Each assembled module will be tested in regard of certain acceptance criteria such as a limited number of bad strips. Moreover, it will be subjected to a thermal cycle (cooling down and heating up) to verify the robustness of the bond wires.

# Chapter 4

# Strip Tracker Electronics

The requirements of the readout electronics for CMS and other future high energy physics experiments are pushing the limits of present technology in terms of speed and the amount of data to transfer. All distributed front-end components have to run synchronously with the accelerator clock. Moreover, as the time of flight of particles has to be considered, clock and trigger delay have to be adjusted locally. Thus, the overall timing synchronization is a very challenging task.

The CMS Silicon Strip Tracker electronics essentially consists of two large blocks. The one-way readout chain transmits the measured data from the detectors to the control room. On the other hand, the bi-directional control chain has to deliver clock and trigger signals to each detector and exchanges control information between control room and front-end electronics such as configuration parameters or temperature monitoring.

In CMS, the read-out information is conveyed in analog state, while the control data are purely digital. All signals are transmitted trough 100 m of optical fibers between front-end and control room. On either end, the light information is converted to electrical signals and vice versa.

Fig. 4.1 shows a sketch of the CMS Silicon Strip Tracker electronics. The readout (top half) and control (bottom half) parts both include components close to the detectors at the front-end (left half) and in the control room (right half).

The Timing, Trigger and Control (TTC) System, which is a common development for all LHC experiments, takes care of clock and trigger distribution through optical fibers. Local receiver boards (TTCrx) provide these signals for the electronic modules. The Front-End Controller (FEC) takes this information, adds specific control signals received over its VME bus interface and sends these data to the front-end control module using a digital optical link. The Communication and Control Unit (CCU) interprets the received information and passes it on to the front-end module. Temperature, voltages and currents are monitored by the Detector Control Unit (DCU). Its data are transmitted to the CCU, which sends it back to the FEC. The PLL (phase-locked loop) delay chip is used for adjusting clock phase and trigger delay. In the readout path, the analog data coming from two APV25 front-end amplifiers are multiplexed onto a single line by the APVMUX chip and sent over the analog optical link. This data are then digitized and pre-processed by the Front-End Driver (FED), which receives the TTC clock and trigger signals as well. It buffers the incoming data and passes them on to a computer farm for further processing.

The CMS tracker uses the $I^2C$ bus, which was developed by Philips [45], for slow control

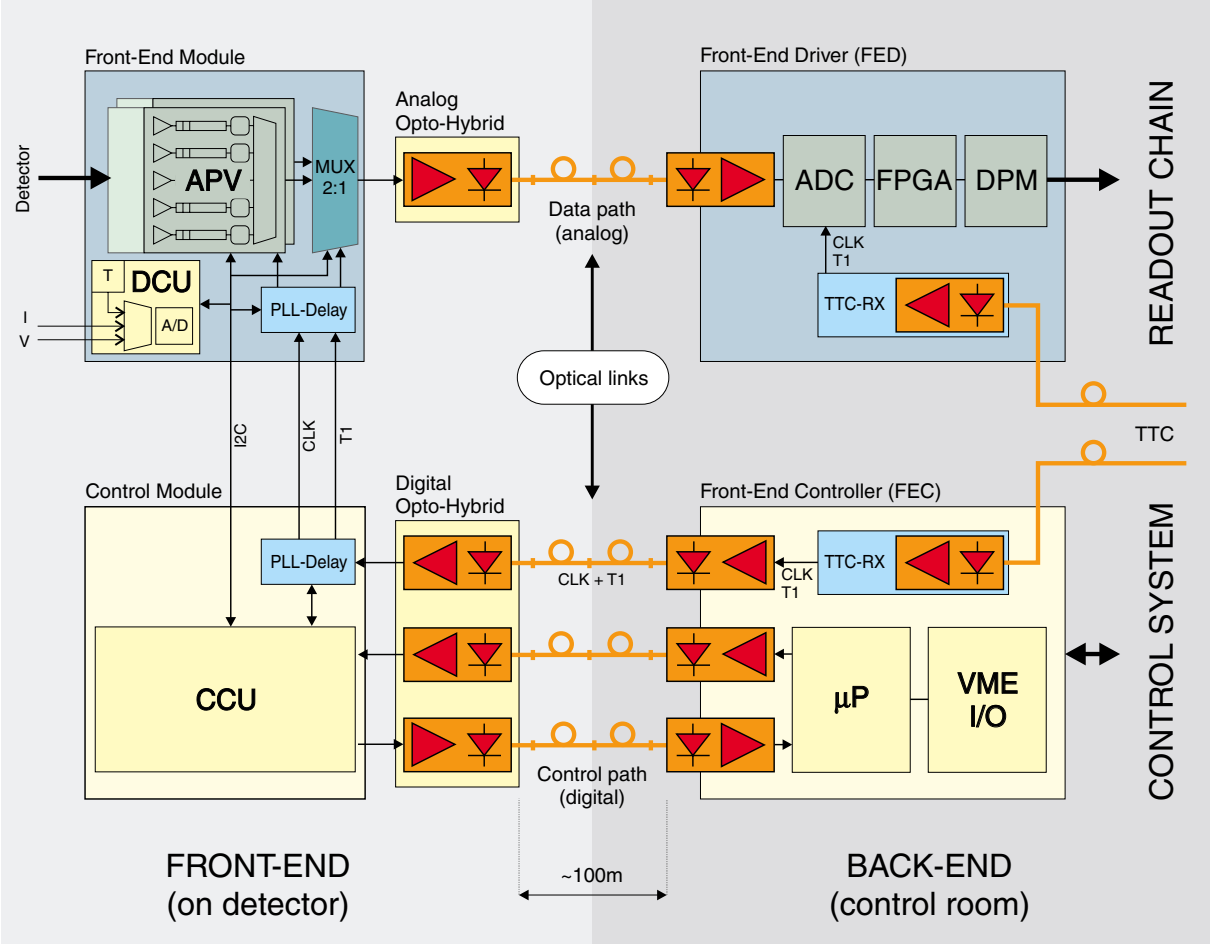



Figure 4.1: The building blocks of the CMS silicon strip tracker readout (top half) and control (bottom half) system. The front-end (left half) and back-end (right half) parts are connected with optical links.

in the front-end. Clock delay settings, configuration parameters or monitored temperatures are transmitted over this bus. An address is assigned to each device on this bus by tying dedicated input pads low or high. Clock and trigger signals are transmitted with low voltage differential signaling (LVDS) levels. In the control room back-end, there is no need for radiation hardness, and the electronic modules are based on the industry-standard VME bus system.

Several ASICs have been developed for the front-end electronics. Since the chips are located close to the detector modules, they have to withstand the same radiation levels. All ASICs are fabricated in the IBM 0.25 $\mu$m deep submicron CMOS process [37], which tolerates radiation far beyond the expected CMS levels.

The trigger line is not only used for the distribution of the first-level trigger, but also for reset and calibration requests. The speed of the trigger line is 40 Mbit/s with the valid symbols given in tab. 4.1. A single logic 1 bit is a trigger, while 101 resets the target components and the calibration request 11 generates an internal calibration pulse in the APV chip. This scheme implies that the minimum distance between two subsequent triggers is three clock cycles, i.e. 1001 and a short dead time of 50 ns is introduced.

The various components of the Silicon Strip Tracker and the APV chip in particular will be

| Symbol | Meaning |
|---|---|
| 1 | Trigger |
| 101 | Reset |
| 11 | Calibration |

Table 4.1: Symbols transmitted over the trigger line.

discussed in detail in the following sections.

## 4.1 APV

The APV chip series was developed as a front-end amplifier for the CMS silicon strip tracker. It includes a preamplifier and shaper, an analog pipeline and a deconvolution filter for each of its 128 channels.

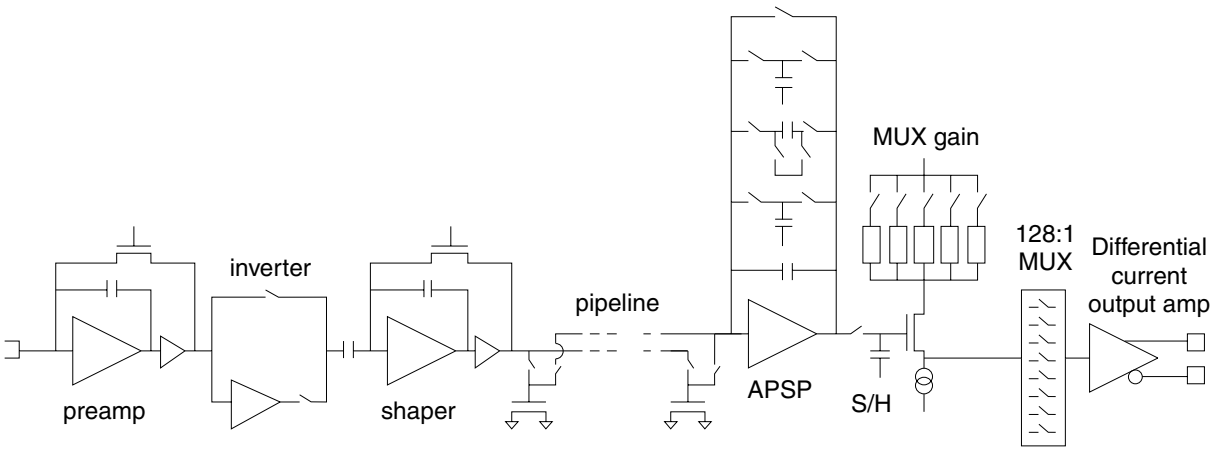



Figure 4.2: Block diagram of the APV chip. The schematics to the left of the 128:1 multiplexer (MUX) is implemented individually for each of the 128 channels.

Fig. 4.2 shows the internals of the APV chip [46]. After the integrating preamplifier, the signal polarity can be selected by optionally inserting an inverter. The CR-RC shaper has a peaking time of 50 ns. Feedback resistors of both preamplifier and shaper as well as bias currents and voltages are programmable. The output of the shaper is sampled with the bunch crossing frequency of 40 MHz (corresponding to a period of 25 ns) and fed into a pipeline of adjustable length. At the end of the pipeline, the signals are extracted upon a trigger request. When the chip is configured for deconvolution, a switched capacitor filter (APSP) performs the three-weight deconvolution method as described in section 2.6.3, p. 35. Alternatively, a single sample of the shaper output is extracted directly. A sample/hold (S/H) stage and an amplifier with programmable gain follow. Finally, the signals of all 128 channels are multiplexed onto a single line with a differential current amplifier output. Moreover, an internal calibration circuit allows to test the functionality of each channel.

The current and final version of the APV chip series is called APV25S1, which is manufactured in the 0.25 $\mu$m submicron process as its predecessor APV25S0. The earlier APV6 version [47] basically had the same functionality, but was produced in the Harris AVLSIRA pro-

cess. There were also a DMILL version called APVD and an adapted APVM chip with longer shaping time and current monitoring capabilities for MSGC readout. The following enumeration gives an overview of the APV chip development [48].

- 1.2 $\mu$m Harris AVLSIRA radiation hard CMOS
  - 1993 – **APV3** – 32 channel pipeline chip implementing CMS architecture of CR-RC shaping and 3-weight deconvolution signal processing.
  - 1995 – **APV5** – 128 channels with addition of analog multiplexer
  - 1996 – **APV6** – 128 channels with analog multiplexer, bias generator, calibration control, and $I^2C$ interface. Full CMS read-out functionality.
  - 1998 – **APVM** – Development of APV6 into MSGC read-out chip
- 0.8 $\mu$m TEMIC DMILL radiation hard CMOS
  - 1997-99 – **APVD** – development of DMILL versions
- 0.25 $\mu$m IBM Deep Submicron CMOS
  - 1999-2000 – **APV25** – Redesign

The most important distinction between the APV25 and its predecessors is a significantly improved noise performance. Moreover, the number of pipeline cells was increased from 160 to 192. Nonetheless, the die size could be decreased due to the smaller structures of the submicron process (fig. 4.3). Moreover, this transition implied a reduction in the supply voltages from $\pm 2.0\,\mathrm{V}$ (APV6) to $\pm 1.25\,\mathrm{V}$ (APV25).

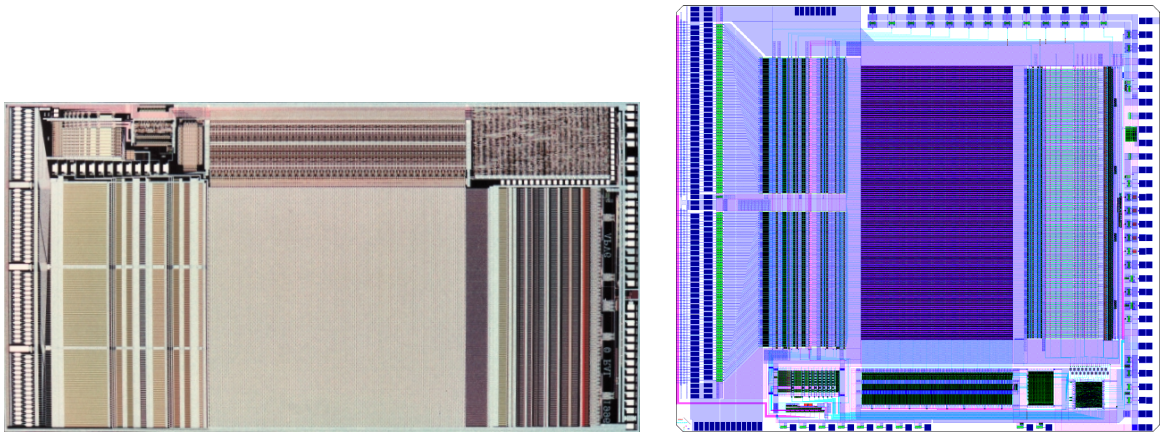


Figure 4.3: The die layout of APV6 ($12.0 \times 6.25\,\mathrm{mm}^2$, left) and APV25S1 ($8.055 \times 7.1\,\mathrm{mm}^2$, right) front-end chips. Both chips are shown seven times larger than in reality. The 128 input pads are visible on the left edges, the large central parts are covered by the pipeline and the control and output pads are to the right.

### 4.1.1 APV25 Circuit Details

The APV25 has an $I^2C$ interface to program internal registers, such as analog bias voltages and currents, the operational mode (peak or deconvolution), and internal calibration settings.

The intention of bias adjustment is to compensate possible radiation degradation. However, irradiation tests have shown that in fact the effect of radiation at the CMS level on the APV25 chip is almost negligible.

Apart from a "soft" reset by applying a 101 sequence at the trigger input, the APV25 has a dedicated input for a reset signal ("hard" reset), which has the same effect as a power cycle.

Compared to previous versions of the APV chip, the APV25 has a new feature in addition to peak and deconvolution modes. In the multi-peak mode, the three samples which would be used for the deconvolution algorithm are issued untreated as if three consecutive triggers had arrived (which is not possible because of the special symbols shown in tab. 4.1, p. 51).

Details of the circuit subsystems [49, 50, 51] will be given in the following sections.

#### 4.1.1.1 Preamplifier and Shaper

The integrating preamplifier circuit (fig. 4.4) is composed of a single-ended folded cascode amplifier with a feedback capacitor of 150 fF and an input transistor of pFET type with a size of $W/L = 2000/0.36\,\mu$m. Its large effective width results from a poly-gate structure, where many smaller gates are arranged in parallel [52, 34], since it turns out that such a design is the best choice with respect to intrinsic noise [35]. The nominal bias current of the input stage is 460 $\mu$A.

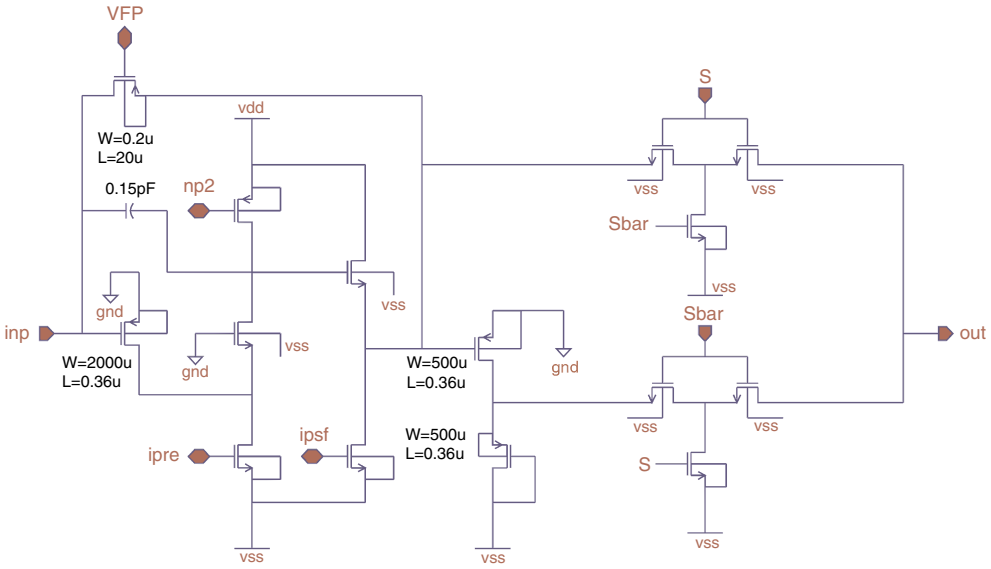



Figure 4.4: Schematics of the APV25 preamplifier.

The output is connected to a source follower, which provides the voltage shift required for stable DC operation through the feedback resistor, which is realized as transistor of variable conductance. As pointed out in section 2.6.2, p. 33, the ohmic feedback avoids drifts and pileup effects. A unity gain inverter follows the preamplifier. With the two mutual switches, either the direct or the inverted output is sent to the shaper stage. While the direct output is intended for use with n-bulk detectors, the inverted output is intended for p-bulk detectors, which produce current pulses of opposite polarity. Since the dynamic range of the shaper is limited, its working point is not centered between the supply voltages. The optional inverter between preamplifier and shaper thus allows linear operation with input signals of either polarity. To avoid parasitic

feedthrough in a switch, the center of the two transistors is pulled to $V_{SS}$ in the off condition. The nominal gain of the preamplifier is 18.7 mV/MIP (1 MIP = 25000 e) with a single channel power consumption of 0.9 mW, which is the predominant contribution of the total chip. Source follower and inverter stages each dissipate 0.125 mW.

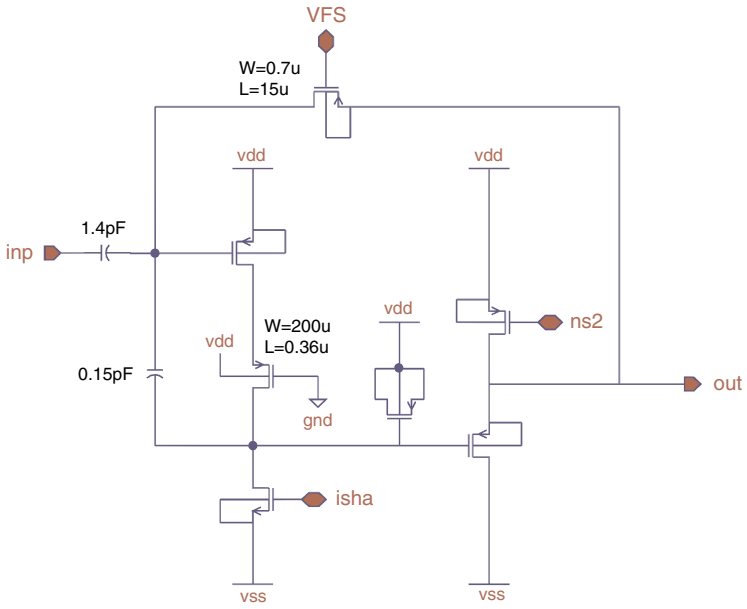



Figure 4.5: Schematics of the APV25 shaper.

The CR-RC shaping filter (fig. 4.5) with a time constant of $T_p = 50$ ns is coupled to the preamplifier output with a 1.4 pF capacitor. It is made of a single-ended non-folded cascode amplifier, again using a feedback capacitor of 150 fF. The input transistor again is of pFET type with the dimensions $W/L = 200/0.36\,\mu$m and a nominal bias current is 50 $\mu$A. Similar to the preamplifier, the feedback resistor is connected to the output of a source follower. The power consumption of a shaper channel is 0.25 mW, equally shared by shaping circuit and source follower, and the overall gain of preamplifier and shaper is 100 mV/MIP.

Fig. 4.6 shows a SPICE simulation of preamplifier and shaper output with an input charge of 0 ... 5 MIPs. The noise performance of the APV chip is determined by the input transistor of the preamplifier. Simulation returned an equivalent noise charge of $\mathrm{ENC_C} = 246\,\mathrm{e} + 36\,\mathrm{e/pF}$, which was confirmed by measurement.

#### 4.1.1.2 Pipeline

The shaper output is sampled at clock intervals and stored in the analog pipeline, which is actually realized as a ring buffer of 192 cells with cycling write and read pointers. Their distance determines the latency time between particle signal and trigger arrival. With a clock frequency of 40 MHz, the maximum time allowed for this trigger decision is more than 4 $\mu$s, well covering the CMS first-level trigger delay of 3.2 $\mu$s. After receiving a trigger, it takes more than 5 $\mu$s to send all pipeline data to the output line through a multiplexer. To protect valuable information from being overwritten, a FIFO with a depth of 32 locations stores the pipeline addresses of those cells waiting for readout. These marked cells are then skipped by the write pointer until the data are actually passed on. In peak mode, only a single sample is retained, which corresponds to the

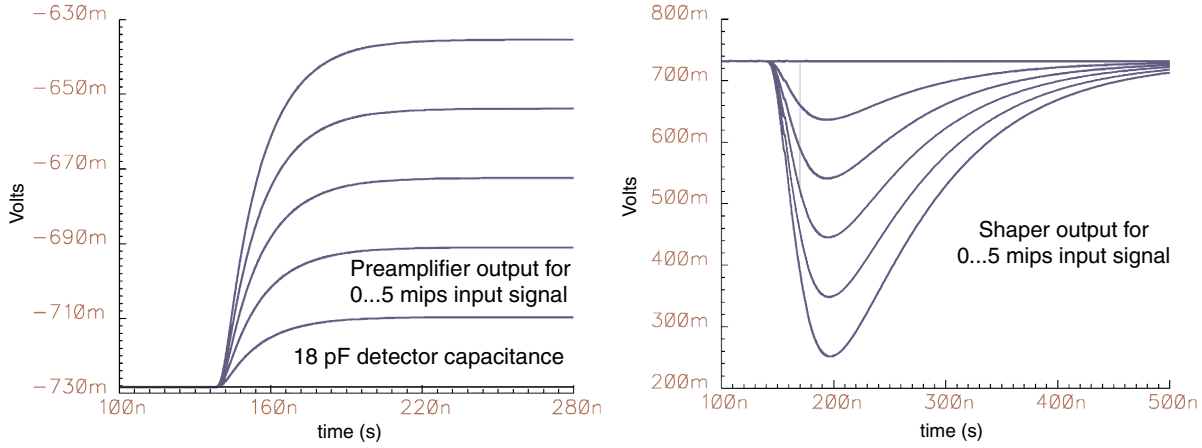



Figure 4.6: SPICE simulation of the APV25 preamplifier (left) and shaper (right) response to an input charge of 0 . . . 5 MIPs (1 MIP = 25000 e).

maximum of the CR-RC shaping curve when clock and trigger latency are properly adjusted. Three cells are marked in deconvolution mode for later processing by the APSP. This procedure avoids dead time while keeping a serial readout scheme.

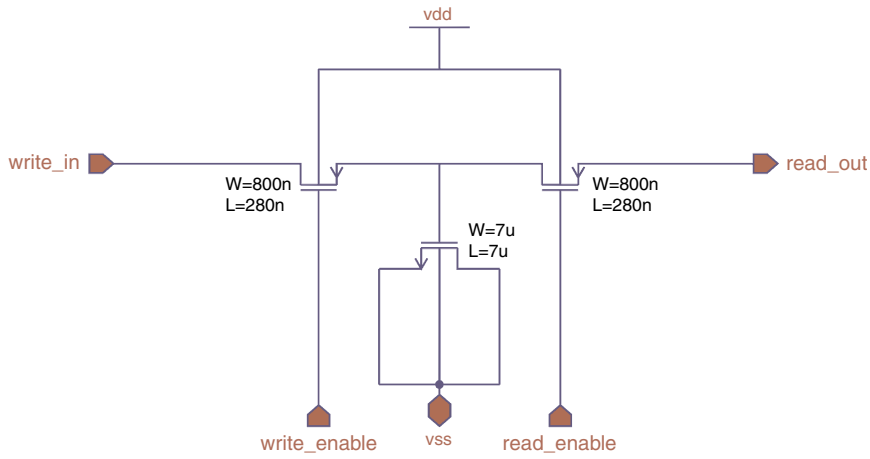



Figure 4.7: Schematics of a single analog pipeline cell of the APV25.

Fig. 4.7 shows one of the 128 × 192 capacitor cells of the APV25. Due to a limitation in the total area of metal-insulator-metal structures allowed within the chip, nFET transistors with the size $W/L = 7/7\,\mu$m are used which have a gate capacitance of 280 fF. These gate capacitors are operated in strong inversion to ensure the best linearity. Normally, the switches on either side of the capacitor are open, only activated by write and read pointers, respectively.

#### 4.1.1.3 APSP

An analog pulse shape processor (APSP) is used to perform the deconvolution algorithm (see section 2.6.3, p. 35). As shown in fig. 4.8, it is composed of a charge amplifier with a switched capacitor network.

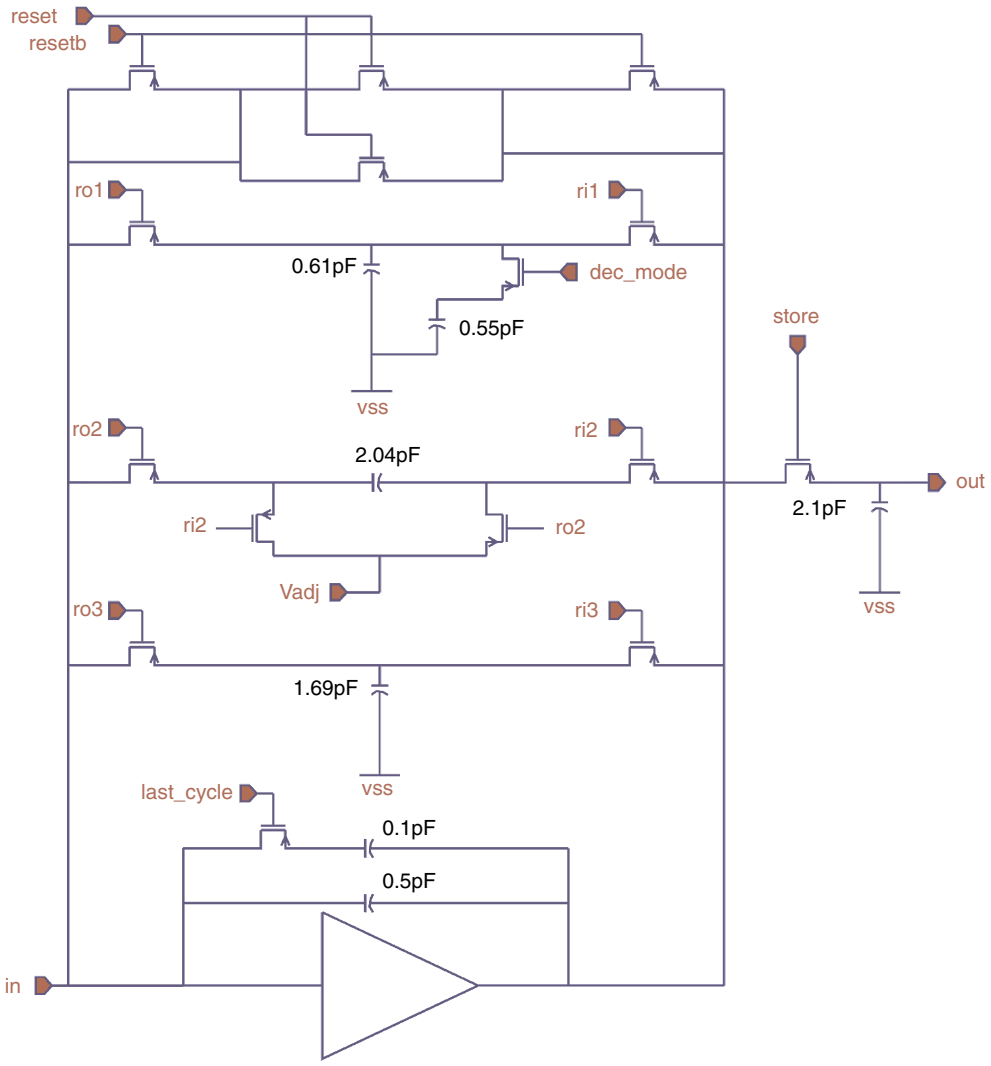



Figure 4.8: Schematics of the APV25 analog pulse shape processor (APSP).

The charge of three samples is converted to a voltage and consecutively stored onto three capacitors (shown in the center between ro and ri switches). Their sizes and thus the stored charges scale with the three weights used in the deconvolution method. Finally, all charges are added and the resulting voltage is applied to the sample/hold circuit. The second capacitor is discharged in reverse polarity as the corresponding weight is negative. In peak mode, only the first capacitor is charged with the single sample, while the second capacitor is used to subtract the APSP reset level, resulting in the same pedestal voltage level in either mode. Moreover, the first capacitor is smaller in peak mode to achieve the same gain as in deconvolution mode.

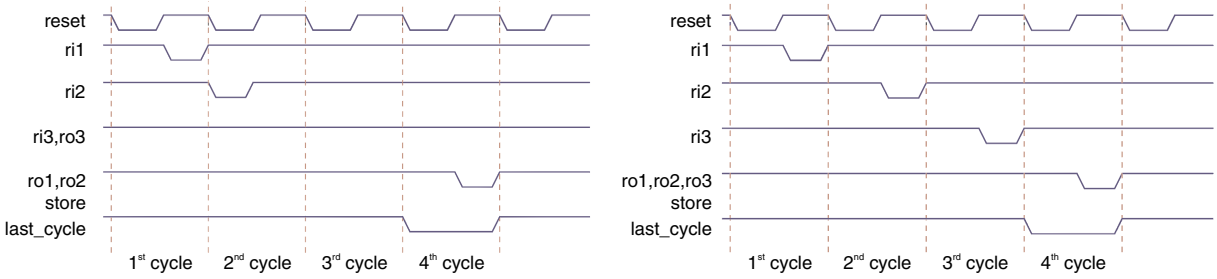



Figure 4.9: Timing of the switches in the APSP in peak (left) and deconvolution (right) modes.

Fig. 4.9 shows the sequence in which the switches are operated for both peak (left) and deconvolution (right) modes. The reset frequency driving the APSP circuit is 1/70 of the system clock. Thus, the chip output signals are always synchronous to the APSP reset, regardless of the arrival time of a trigger signal.

One APSP channel consumes 0.2 mW of power. The overall gain of the analog chain is 100 mV/MIP with a nonlinearity of less than 0.6% and 2% over a 5 MIP range in peak and deconvolution modes, respectively. The noise in deconvolution mode is higher than in peak mode because the rising edge of the shaper output, which is used for the third sample, is subjected to slewing effects for large signals.

#### 4.1.1.4 Multiplexer and Output Buffer

The sampled output of the APSP is sent to a single output line through a three-stage multiplexer. Its principle is shown in fig. 4.10. Due to the staged multiplexing, the output order of the 128 channels does not correspond to the natural channel order. The following calculation must be performed to retrieve the physical channel number $c$ from output sample number $n$:

$$c = 32\,(n \bmod 4) + 8\,\mathrm{int}\left(\frac{n}{4}\right) - 31\,\mathrm{int}\left(\frac{n}{16}\right) \tag{4.1}$$

Fig. 4.11 shows the multiplexer circuit. The APSP output voltage is first converted into a current, which allows faster and more linear switching with less crosstalk. The conductance of the input stage can be selected by switching on or off several parallel resistors. This allows trimming of the multiplexer gain since the accuracy of chip internal resistors is limited to about 20%. Channels which are not switched through have their currents dumped into a dummy load. This is a waste of power but ensures that the voltages are not affected by the switching procedure. To the bottom right of fig. 4.11, a circuit which inserts digital signals to the output line, is shown. The digital logic levels are $\pm 400\,\mu$A.

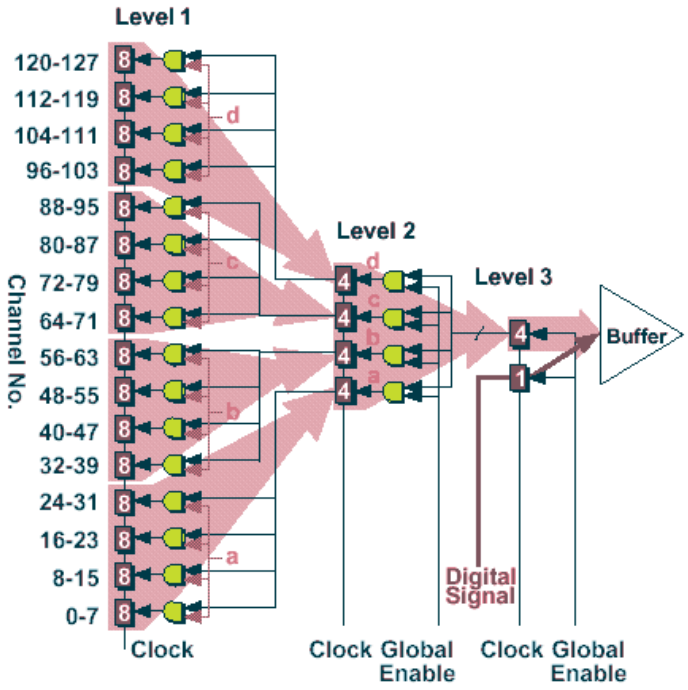



Figure 4.10: Principal structure of the APV25 multiplexer.

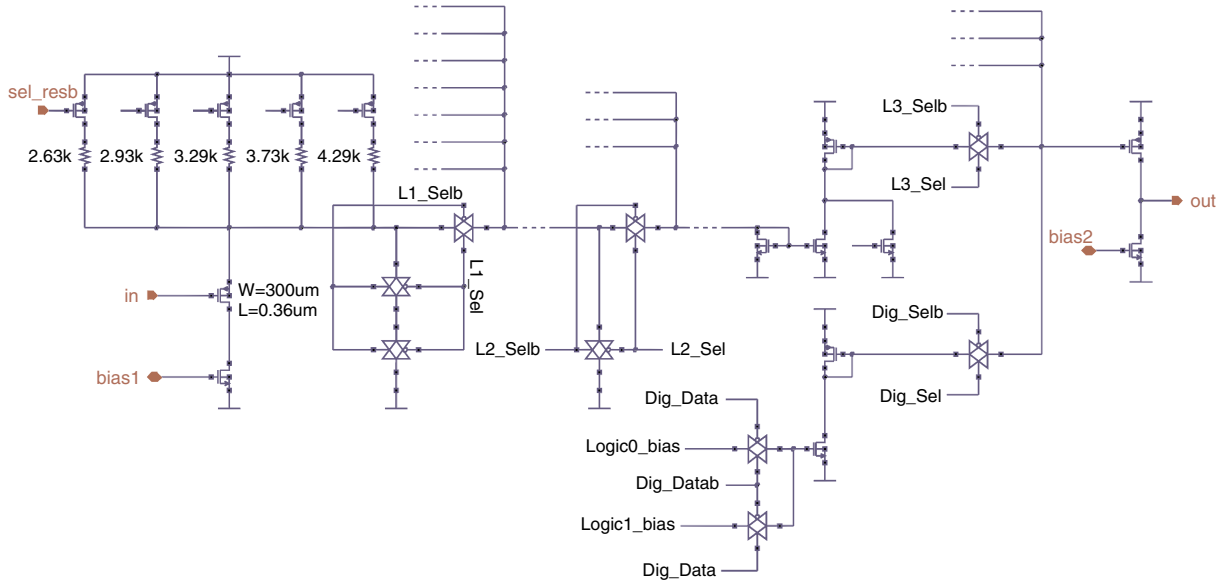



Figure 4.11: Schematics of the APV25 multiplexer.

The analog gain at the output of the multiplexer is 100 $\mu$A/MIP and the power consumption of the whole multiplexer is 22 mW at the nominal input bias current of 50 $\mu$A.

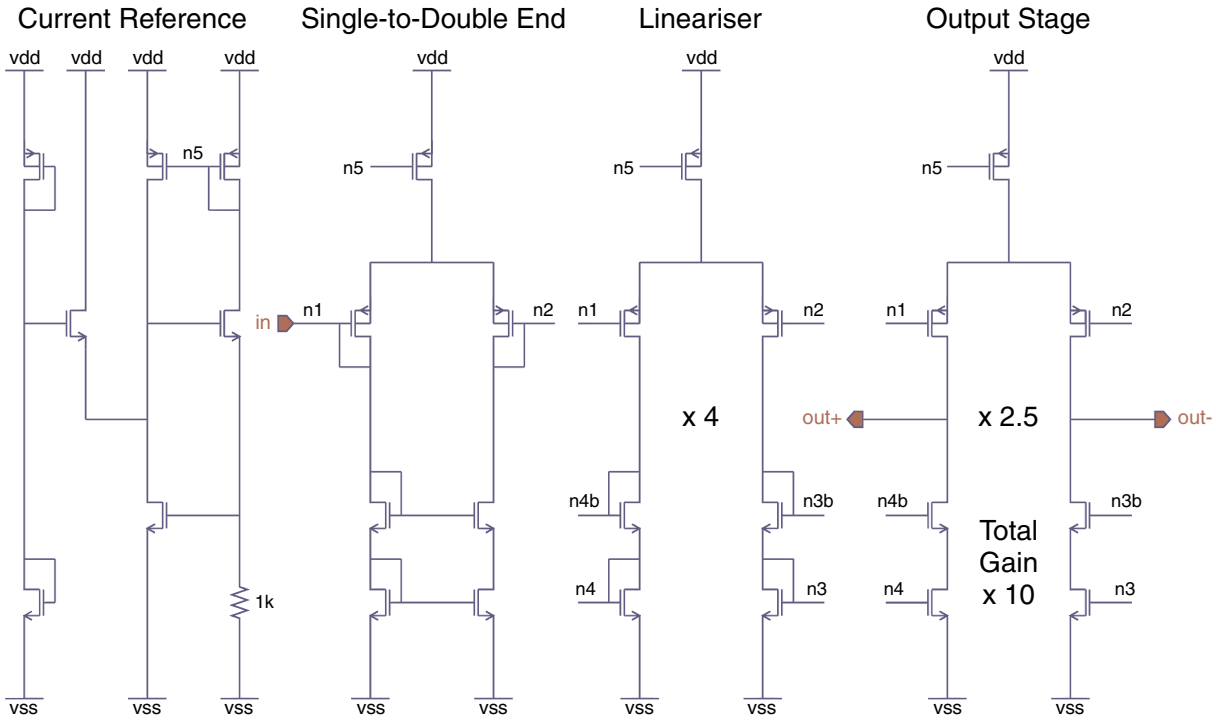



Figure 4.12: Schematics of the APV25 output buffer.

The output buffer shown in fig. 4.12 finally amplifies the multiplexer output current and splits it into differential channels. Both output lines have an analog gain of 1 mA/MIP, resulting in a differential signal of 2 mA/MIP and differential logic levels of $\pm$8 mA. The output buffer power consumption is 20 mW.

#### 4.1.1.5 Internal Calibration

The APV25 includes an internal calibration generator [53], which allows to check the functionality of each channel. The operational principle is to apply a voltage step pulse $\Delta V$ to a series capacitor $C$ which is connected to the preamplifier input. The injected charge $\Delta Q$ is determined by

$$\Delta Q = C\,\Delta V \quad . \tag{4.2}$$

The calibration pulses can be applied to one (or more) out of eight groups, each connected to 16 input channels of the amplifier. This selection is done by a mask register which is programmable over the $I^2C$ bus. Also the amplitude of the voltage step and thus the injected charge can be adjusted. Moreover, the timing of the pulse can be adjusted in steps of 1/8 of the system clock (3.125 ns at 40 MHz).

Fig. 4.13 shows the scheme of the APV25 calibration delay circuit and the mask register for the selection of a group of input channels into which the charge is injected. The delay line has 16 stages with a tapping on one of the centered eight. Each stage is implemented as a current-starved inverter followed by a Schmitt trigger. A Delay-Locked Loop (DLL) circuit controls the

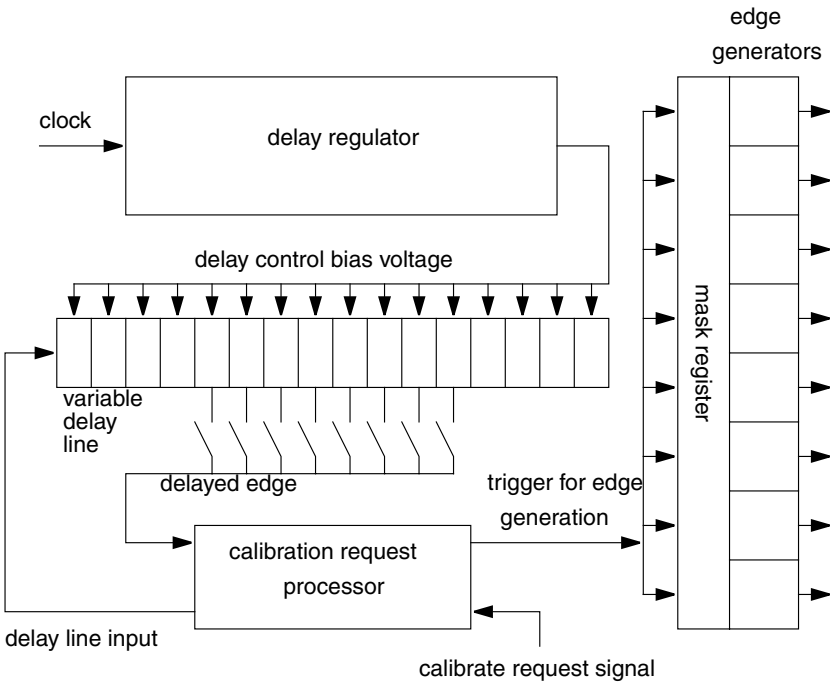



Figure 4.13: Block diagram of the APV25 calibration delay circuit and the mask register.

current bias of the elements to ensure that the total delay of all 16 stages equals two system clock periods.

The output stage of the calibration circuit for a single channel is shown in fig. 4.14. With each calibration request signal, the state of the calibration trigger line is toggled if enabled for that particular channel on the mask register. The amplitude of the voltage pulse is adjusted with the programmable bias, driving the current source of the complementary switching stage. The current source can be completely switched off to avoid possible crosstalk. The coupling capacitor is implemented in between two metal layers of the routing lines on the chip.

The current source generates a nominal current between 0 and 255 $\mu$A, resulting in an injected charge of 0 to 25.5 fC. However, since both the resistors defining the amplitude of the voltage step and the capacitor have considerable tolerances, the charge is not very well defined.

Fig. 4.15 shows the timing of the APV25 internal calibration. A calibration request (cal_req) is detected when a 11 symbol appears on the trigger line. Then this signal is sent to the delay line (req_in), where the tapped output (req_out) is returned after a variable delay time td. Finally, the calibration switch is toggled, injecting charge into the selected channels. The amplifier detects this signal, resulting in the shaper output as shown.

A calibration request only generates a charge signal, but it does not trigger the APV readout. Thus, a normal trigger must be issued after the calibration request, separated by the latency time plus a small offset determined by the calibration delay circuit. Since the calibration edge is toggled after each calibration request, the signal polarity does the same. To receive a series of unipolar signals, one should periodically send the sequence 11 – 1 – 11 on the trigger line, where the second calibration request (which is not followed by a trigger) dumps the signal of unwanted polarity.

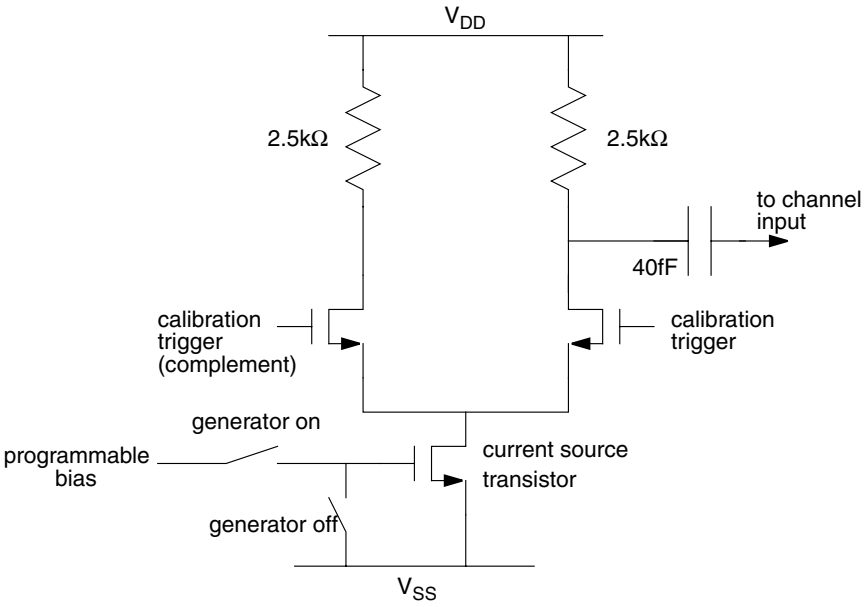



Figure 4.14: APV25 calibration edge generator circuit.

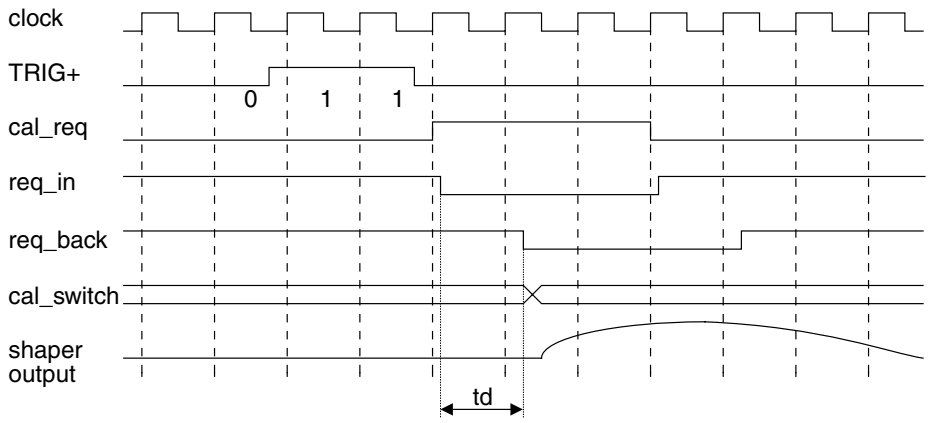



Figure 4.15: Timing diagram of the APV25 internal calibration. td is the variable delay time.

### 4.1.2 APV25 Output

The output of the APV25 is normally clocked with half the system clock (20 MHz), but can be switched to 40 MHz. When no data are pending, the output is at logic low level (−8 mA differential current). Synchronization pulses ("tick marks"), which are derived from the APSP reset, are issued every 70 system clock cycles. These pulses are useful for debugging purposes: When tick marks appear on the output, one can be sure that the chip is alive and correctly receives the input clock.

After receiving a trigger, the APSP needs $4 \times 70$ clock cycles for data processing (see section 4.1.1.3, p. 55). Then, a data frame is sent to the output, starting at the position where a tick mark would be issued otherwise. Fig. 4.16 shows such a frame, which starts with a header of three bits with logic high level. The readout processor can thus identify a data frame by searching for at least two samples of logic high level in the output stream.

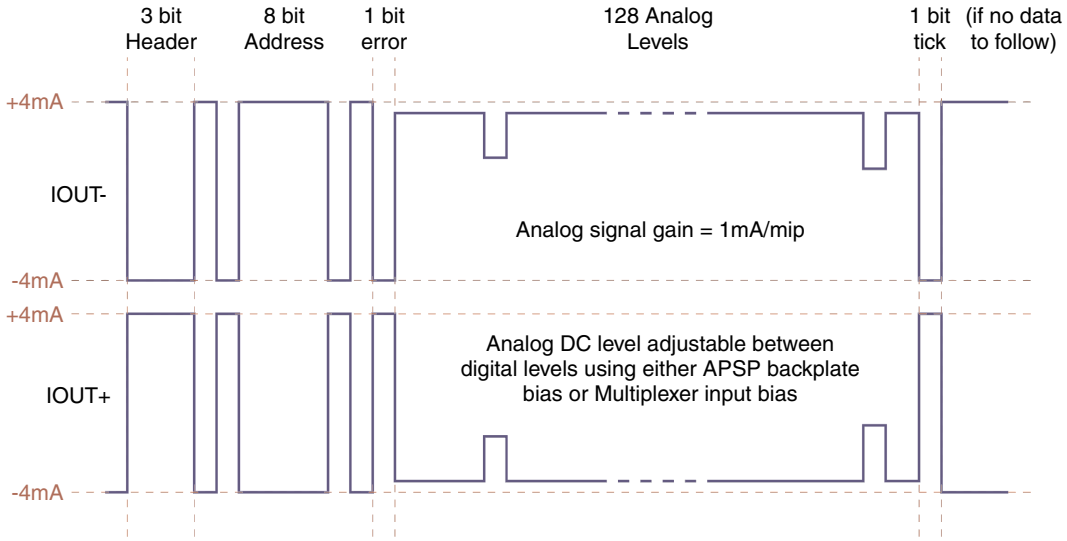



Figure 4.16: Schematics of the APV25 output buffer.

An eight bit address identifying the pipeline cell follows. The pipeline column locations are numbered in a specific scheme inspired by the Gray Code. A set of chips running on the same clock and trigger lines ought to have synchronous pipeline addresses, allowing to identify a chip error (e.g., by a single event upset, see section 5.1.6, p. 99), by an address mismatch. Moreover, the address can be used to tag the output data in case of a known bad pipeline location.

After the address, a single bit is sent which may indicate an error. The internal chip logic watches read and write pointers of the pipeline buffer and checks if their distance equals the latency setting. If this is not the case, a "latency error" occurred and the error bit is set. Moreover, a "FIFO error" is produced when the FIFO, which stores the addresses of pipeline cells containing data to be read out, is full. After sensing an error in the data frame, the type of error can be read over the $I^2C$ bus. Errors are cleared by a (soft or hard) reset applied to the APV25.

After header, address and error bit, the analog data of all 128 channels are transmitted in multiplexed order. The overall output is 140 bits wide. With 20 MHz or 40 MHz output modes, the output frame exactly replaces four or two tick marks including the interval following the pulse. Thus, a tick mark follows immediately after an output frame except when another trigger

is pending. In that case, the first data frame is immediately followed by another one.

## 4.2 Front-End Electronics

Several ASICs support the APV readout chip in the front-end. In the readout path, the APV-MUX is used to multiplex the output of two APV25 chips onto a single transmission channel. On the control and monitoring side [54], the PLL-Delay splits clock and trigger signals from a common line and is used to fine-tune clock and trigger delay. The DCU monitors voltages, currents and temperature. Finally, the CCU is responsible for the communication with the control room and acts as an $I^2C$ bus master. Since FEC and CCU are a logical unit, they will be discussed together in a later section.

### 4.2.1 APVMUX

A CMS silicon strip detector module includes four or six APV25S1 chips and one APVMUX chip [51] to multiplex the output of APV pairs together onto a single line. Thus, the APVMUX core is a set of fast switches.

The APV clock is 40 MHz, but the output is only clocked with 20 MHz. After a 101 reset sequence, the output begins on even or odd system clock periods, depending on whether the $I^2C$ address of that chip is even or odd. Thus, the output frame of odd chips is delayed by 25 ns with respect to even chips. This allows the APVMUX to switch between even and odd chips, presenting the stable second half of each sample. This scheme is illustrated by fig. 4.17.

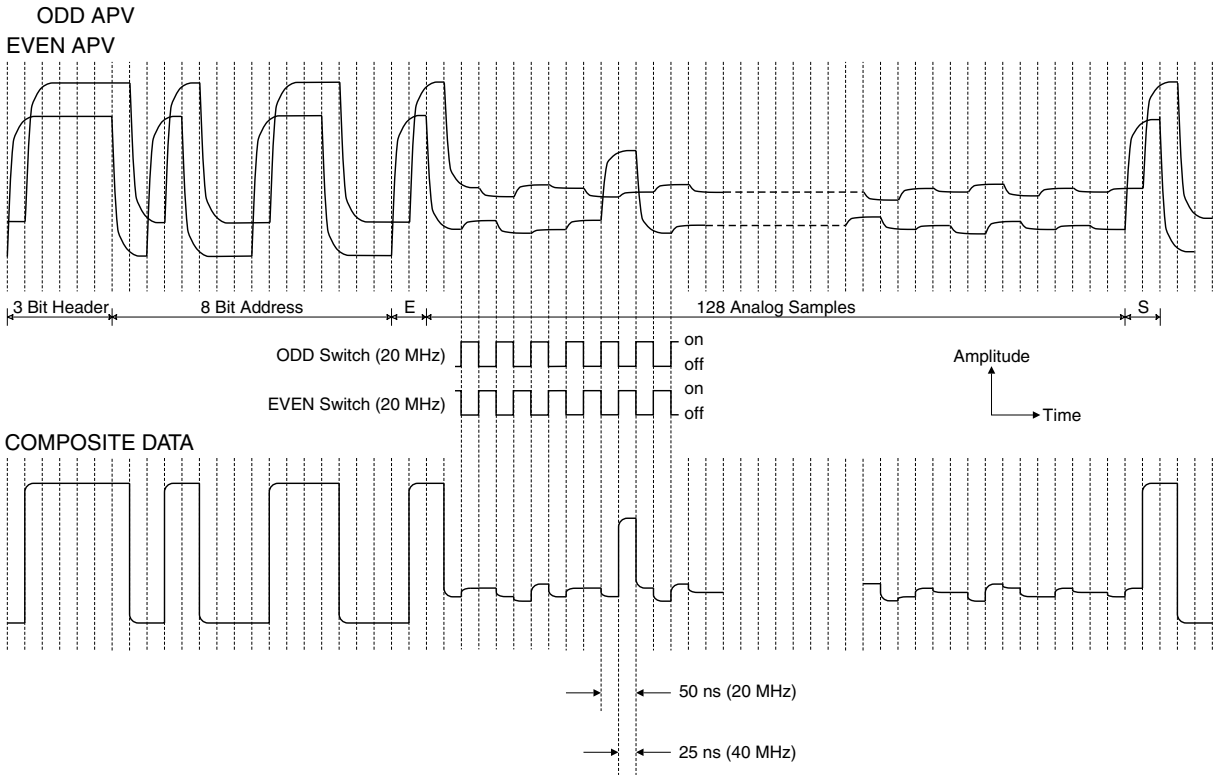



Figure 4.17: APVMUX switching between two APV25 output lines.

The APVMUX includes an $I^2C$ interface for choosing different termination resistors. By default, each input is terminated with 50 Ω against the center voltage. Apart from the switching circuit, the APVMUX chip also includes a full implementation of the PLL-Delay described in the following section.

### 4.2.2 PLL-Delay

The PLL-Delay chip has to provide clock and trigger signals with adjustable delay. Both signals are propagated to the front-end on a single line. They are mixed such that a clock pulse is omitted when a trigger occurs as shown in fig. 4.18

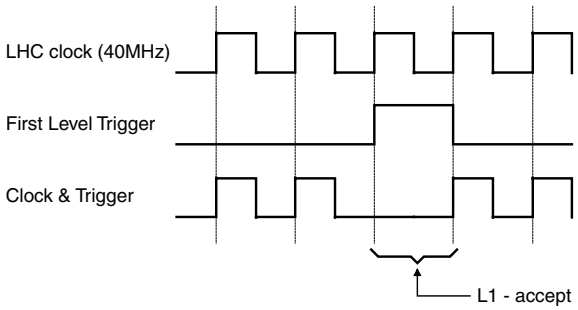



Figure 4.18: Clock and trigger signals and their combination, which is used to transmit both signals over a single line between control room and front-end.

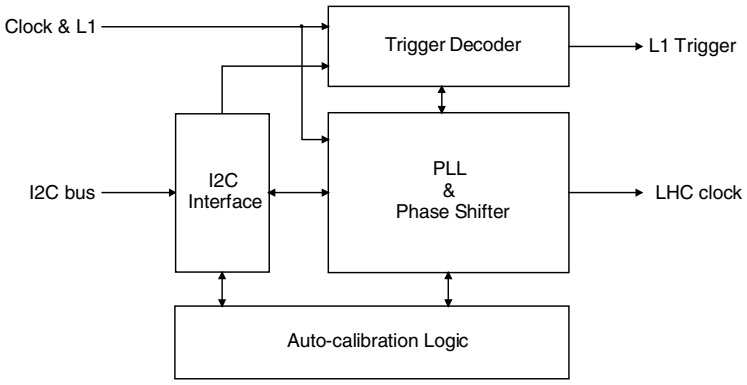



Figure 4.19: Block diagram of the PLL-Delay chip.

Fig. 4.19 displays the building blocks of the PLL-Delay. To restore the full clock without missing pulses, a phase-locked loop circuit is employed as indicated by the name of chip. The difference between input and output signals of the PLL is the recovered trigger. Moreover, the circuit includes a clock phase shifter. This task is performed by a voltage controlled oscillator (VCO) composed of 12 delay cells which generate 12 different clock phases evenly distributed within half a clock period. These phases are inverted to fill the other half period, while an automatic calibration unit tunes the PLL circuit. Thus, 24 taps are offered to select a fine delay in steps of 1.04 ns within a clock cycle. Additionally, a coarse delay can retard clock and trigger signals for up to 15 clock cycles.

Fine and coarse delay are programmable over the $I^2C$ interface. For protection against single event upsets (SEUs) caused by the radiation, the PLL-Delay uses triple-voting. Thus, a memory

cell value is validated by the majority vote of three single cells. When a mismatch between three such cells is encountered, a status register is set which can be read by $I^2C$. In that case, the chip is still fully functional but the next SEU occurring on the same cell triplet will definitely cause an unwanted condition. To avoid such an error, the chip should be reprogrammed soon after a SEU is indicated in the status register.

### 4.2.3 DCU

The Detector Control Unit is monitoring low voltages, the detector current and temperature. Fig. 4.20 shows the its function on a silicon detector module. A small resistor is inserted in the ground connection of the polysilicon resistors to measure the voltage drop which scales with the detector leakage current. Four equal resistors between the supply rails, tapped at VDD/2 and VSS/2, are used to monitor the supply voltages. Moreover, an external NTC thermistor measures the silicon detector temperature, while an integrated temperature sensor monitors the DCU chip temperature.

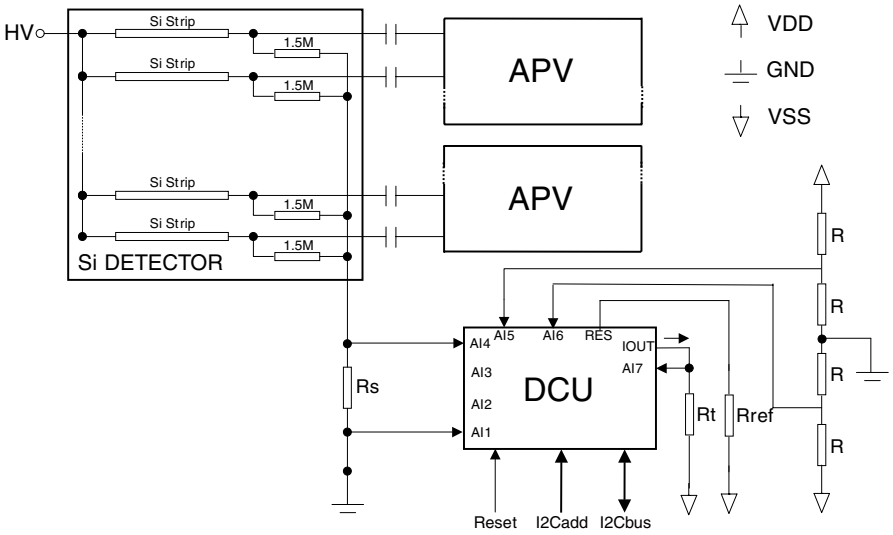



Figure 4.20: Connections of the DCU on a silicon detector module.

The DCU architecture is shown in fig. 4.21. Seven inputs and the internal temperature sensor are multiplexed onto an ADC with 12 or optionally 14 bits resolution. The reference voltage for the ADC is generated normally from an internal bandgap diode, but can be overridden by an external source for test purposes. The ADC is implemented in a single slope serial architecture, where a linear ramp is obtained by charging or discharging a capacitor with a constant current. The analog input voltage is compared with the linear ramp and a counter, which is fed from the 40 MHz system clock, and stops at the trip point of a comparator. A possible offset is compensated by averaging two consecutive measurements with opposite slopes. Thus, a digitization with 14 bits resolution can be achieved with a sampling time shorter than 1 ms. The ADC allows rail-to-rail input due to a complementary discriminator stage. The negative input range is covered by a pFET based discriminator, while an nFET type takes care of positive input. The ADC control and readout is done by the $I^2C$ interface. Similar to the PLL-Delay, the digital logic is designed for triple-voting to withstand SEUs.

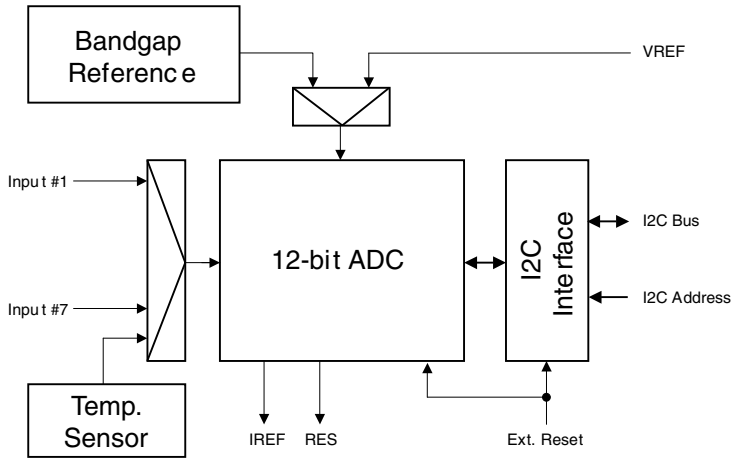



Figure 4.21: Block diagram of the DCU.

## 4.3 Optical Links

In the CMS tracker, optical fibers are advantageous compared to copper cable in several aspects: First of all, they place much less material within the tracker volume, minimizing unwanted multiple scattering and interaction probability. There are no problems with shielding and ground loops, since no electric connection is needed between transmitter and receiver. However, optical transmission is much more expensive than simple cabling, and optical connectors are not as robust as their electrical counterparts. Nevertheless, CMS has decided to use optical links for both digital and analog signal transmission.

Common specifications have been defined for the optical links within CMS, which include:

- 1310 nm wavelength
- Edge-emitting semiconductor lasers
- Single-mode fibers
- 40 MHz clocked transmission

The choice of the wavelength and the limited space imply the use of edge-emitting semiconductors. Multi-Quantum-Well (MQW) InGaAsP edge-emitting laser diodes have been selected because of their good linearity, low threshold current (below 10 mA) and proven reliability. Photodiodes are epitaxially grown, planar InGaAs devices of small active volume. Both digital and analog signals are transmitted at 40 MHz, which is quite slow compared to the capabilities of modern optoelectronics.

Fig. 4.22 gives an overview of the optical links used in the CMS tracker. Approximately 50000 links are required for the analog readout, while the digital control needs only about 1000 lines. Most of the distance between detector and control room will be covered by 96-way multi-ribbon optical fibers. On a patch panel outside of the CMS experiment, the fibers are split into groups of twelve, leading to the edges of barrel and disk layers. Pigtails, which are attached to each laser and receiver, connect to the 12-way fibers there.

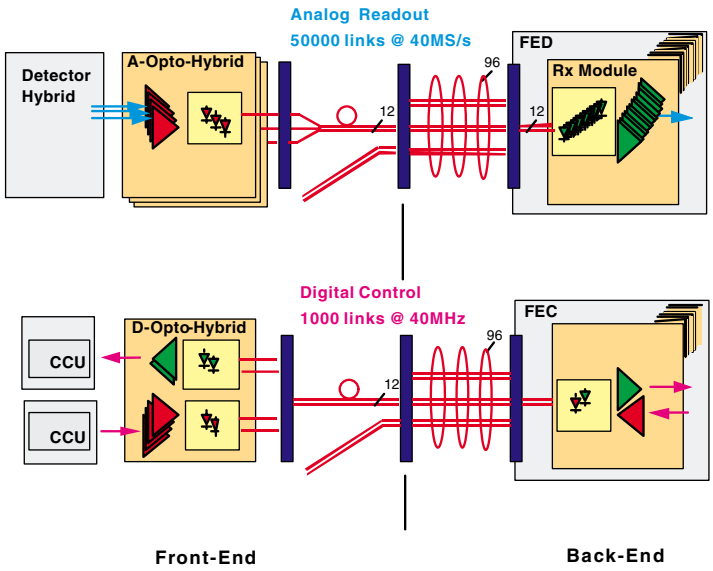



Figure 4.22: Optical links for readout and control in the CMS tracker.

### 4.3.1 Analog Optical Link

The analog optical link is used to transmit the multiplexed APV output to the control room, where it is digitized and processed by the FED.

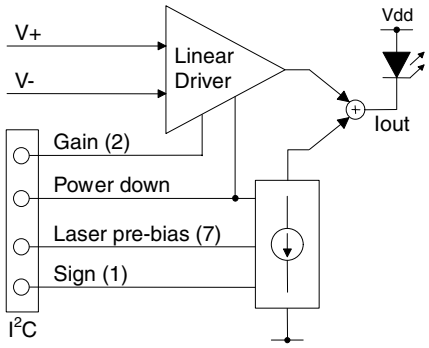



Figure 4.23: Building blocks of the CMS Laser Driver ASIC.

On the transmitter boards (analog optohybrid), two or three lasers are fed by the Laser Driver ASIC [55]. This chip receives analog signals from the APVMUX and converts them to a current suitable for the lasers. The block diagram of the Laser Driver is shown in fig. 4.23. Since the optical output power of semiconductor lasers is zero below a certain threshold, the Laser Driver generates a programmable bias current which is added to the input related current. Typically, a bias current slightly above the threshold is selected for optimum linearity and noise performance at low power consumption. Moreover, four different gains of the amplifier can be selected. The Laser Driver settings are programmed over its $I^2C$ interface. For radiation robustness, the chip internal registers are implemented in triple-voting logic (see section 4.2.2, p. 64) and a readable status register reflects SEU detection.

The radiation to which the transmitters are subjected causes an increase in the laser threshold

and a small reduction in gain. Both effects can be compensated by proper programming of the Laser Driver.

On the receiver side, the optical signal will be detected by a pin diode with an amplifier. These components will be integrated in the FED.

The specifications of the analog optical link are compared with own measurements performed on a prototype link in section 5.2.1, p. 113.

### 4.3.2 Digital Optical Link

The digital optical link uses the same components as the analog link for the transmitter section located in the radiative environment of the experiment. Since two-way communication is required on the control part, pin diodes and a radiation tolerant receiver ASIC [56] will be included on the digital optohybrids as well.

On the control room side however, commercially available optical transceivers will be used. Suitable components have been selected and tested at HEPHY and a prototype was built and presented in early 2001 [57]. Finally, these parts will be included in the FEC.

The best digital signal transmission on fiber optics is obtained with DC balanced data containing the same amount of low and high level bits on average, as it is implicitly the case with the clock. For the data line, this is achieved with a special four to five bit encoding and the NRZI (Non Return to Zero with Invert 1 on change) scheme. Basically, this scheme uses a line transition to represent a "1" and no transition to represent a "0". The idle symbol, which is sent when no other data are pending, is "11111", resulting in a square wave output of half the clock frequency.

## 4.4 Back-End Electronics

### 4.4.1 TTC System

Global clock and trigger signals are needed in virtually all electronic circuits in the LHC accelerator and experiments. Therefore, a common distribution system based on optical fibers has been developed by RD12 [58] at CERN.

The Timing, Trigger and Control (TTC) system consists of various transmitter, fanout and receiver modules. Miniaturized receiver ASICs (TTCrx) will be integrated in FEC and FED.

The TTC transmits two time-multiplexed channels (A and B) at 80 MHz. Channel A is reserved for the first level trigger signal, while channel B can be used for custom purposes. The clock is recovered from signal transitions.

### 4.4.2 FEC and CCU

FEC and CCU are the building blocks of the digital control path of the CMS Silicon Strip Tracker. They are responsible for the transmission of clock and trigger signals from the control room to the front-end electronics. Moreover, control commands and readback values are transmitted in both directions.

The Front-End Controller (FEC) receives the clock and trigger information from an integrated TTCrx receiver. Moreover, it has a control bus interface for communication. The present prototype of the FEC is built in the PMC (PCI Mezzanine Card) form factor with a PCI interface, while the final FEC will be a VME module of 9U height.

A single FEC is connected to a number of Communication and Control Units (CCUs) in a token ring network topology (fig. 4.24). The CCUs in such a ring are located close to each other within the silicon tracker, while the connection to the control room is made through the digital optical link.

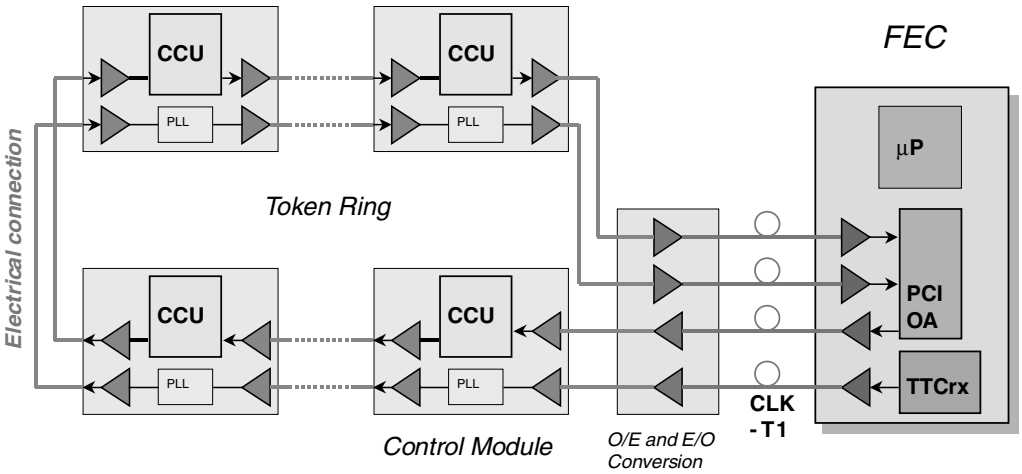



Figure 4.24: The FEC and CCU token ring architecture.

In the ring, a token is initially sent out by the FEC and passed on from one station (CCU) to the next. A node which wants to send data replaces the token by a data frame, which is forwarded until received by the FEC, where the packet is modified and passed on until it returns to the sender. This node verifies the FEC acknowledgement and a checksum. If the transmission was successful, an empty token is inserted in the ring instead of the data frame; otherwise, the data packet is resent.

The token ring architecture minimizes the connections needed between the stations, but relies on the functionality of all links. If a single connection is broken, the whole ring is out of control. To overcome this risk, the final configuration of the CMS tracker control token ring will be redundant in a way that there is a second, staggered ring. Each station will have two interfaces and automatically detect which one is in the currently active ring. Fig. 4.25 shows such a redundant network, which is invulnerable to a single connection or CCU failure.

The building blocks of the CCU are shown in fig. 4.26. The CCU receives the combined clock and trigger signal and passes it on the PLL. Moreover, it implements a 16 channel $I^2C$ bus master used for the slow control and readout in the front-end. It also generates the (hard) reset signal for other chips and includes memory and I/O local bus interfaces, which will not be used in the CMS tracker.

Each CCU module will include a PLL chip for clock and trigger separation. These signals are sent to an LVDS fanout ASIC. Groups of $I^2C$, clock, trigger and reset signals are then distributed to each front-end module through interconnect boards.

### 4.4.3 FED

The Front-End Driver (FED) receives and digitizes the analog data of multiple APVs. Moreover, it extracts the data frames out of the stream and processes the signals.

The current prototype of the FED [59] is realized in the PMC format with eight electrical input channels and a PCI interface. Fig. 4.27 shows the block diagram of the FED-PMC.

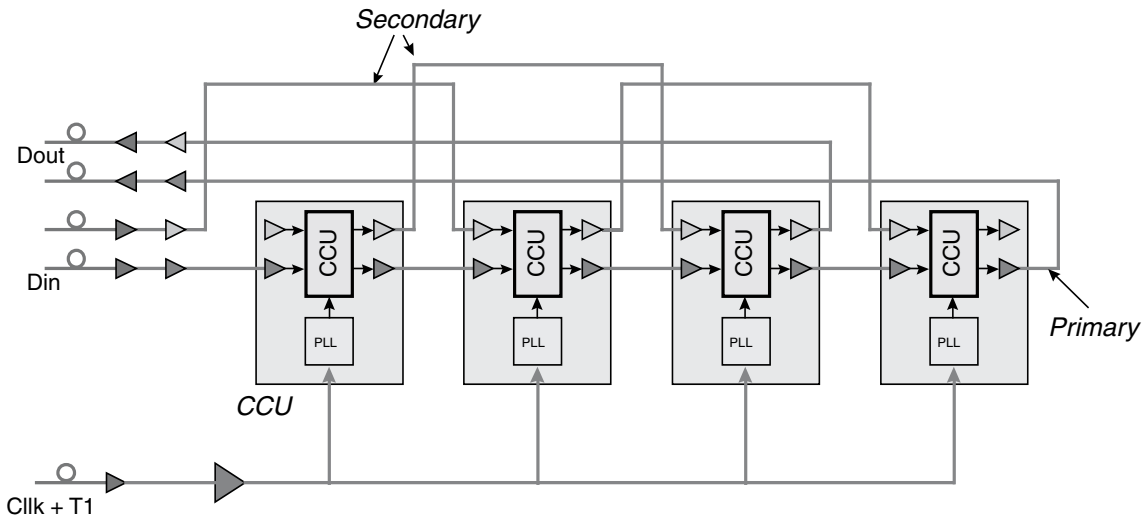



Figure 4.25: Redundant skip-fault architecture of the token ring.

The analog inputs are digitized by 10 bit ADCs (of which 9 bits are read out) at 40 MHz. Similar to the PLL ASIC, the sampling time can be adjusted within a clock period for optimum sampling performance. After a trigger is received, a programmable number of samples is stored in a dual port memory (DPM). The data are then fetched by the Xilinx FPGA unit for further processing. Currently, only the frame search is implemented which extracts header, address, error bit and channel data of an APV frame and passes them on to the PCI interface for readout. In future versions, also signal processing such as channel reordering, pedestal subtraction, common-mode correction, zero-suppression and clustering algorithms will be included in the FPGA to reduce the amount of data.

The final FED will be a 9U VME board including analog optical receivers for 96 channels, a TTCrx receiver for clock and trigger input and a high-speed interface (DAQ link) to the subsequent event builder. The overall input data rate of the final FED will be 3.1 GB/s, which will be condensed to about 100 MB/s at the DAQ link output.

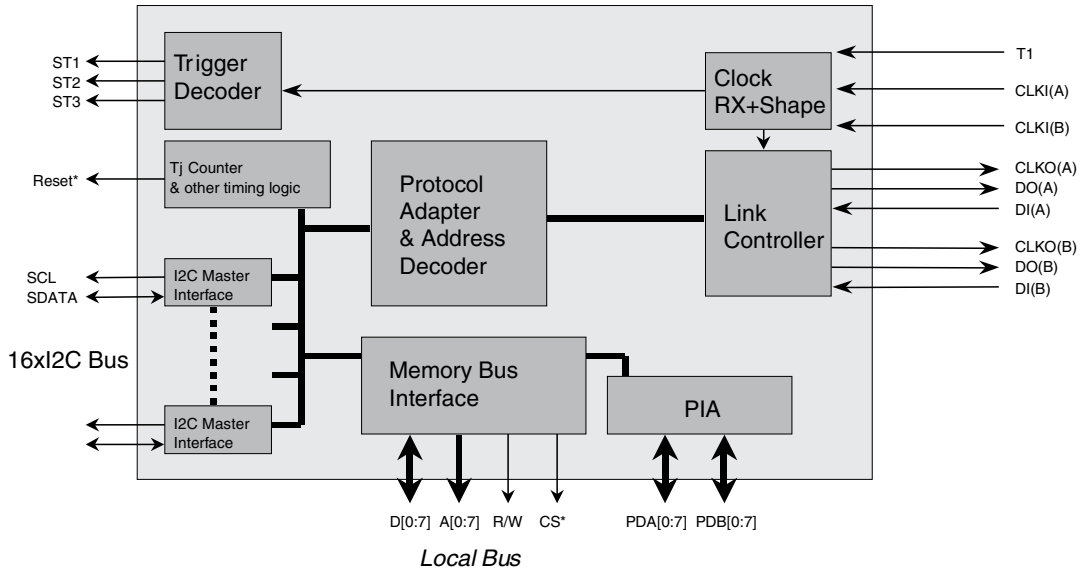



Figure 4.26: Block diagram of the CCU.

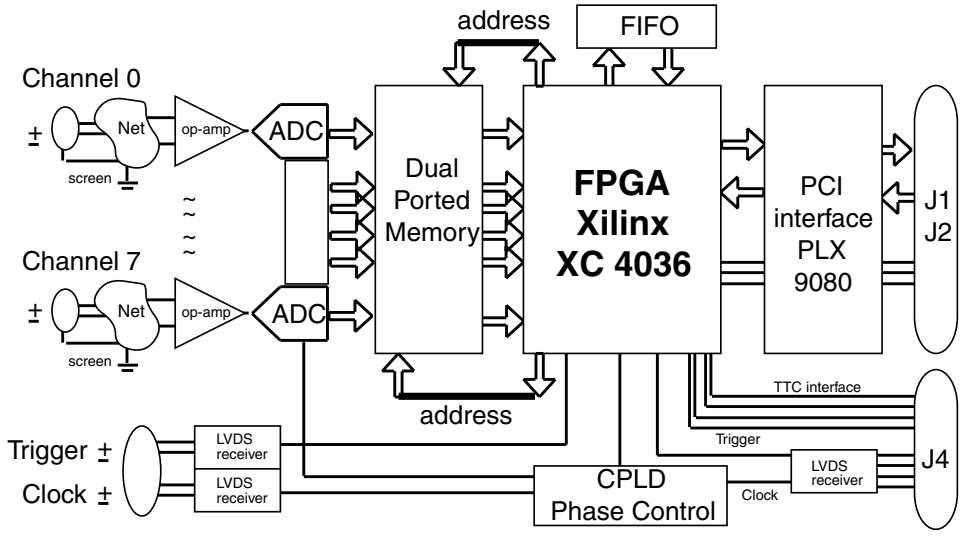



Figure 4.27: Architecture of the FED-PMC prototype.

# Chapter 5

# Experimental Results

This chapter discusses experiments conducted by myself in cooperation with colleagues at HEPHY. Most of my work was devoted to the APV6 and APV25 front-end readout chips and their environment. Therefore, the major part of this chapter is focussed on APV tests.

## 5.1 APV Tests

Although a hybrid with one or more APVs, maybe connected to a silicon detector, does not take much space, the surrounding electronic control and readout modules fill up a rack and also a computer is needed for the data acquisition. Thus, the development of such a chip test system is challenging itself.

Since many of the final readout components described in chapter 4 were not available in the past years (and some still are not), the Electronics II group at HEPHY decided to build a system on their own. The modular VME based system we use now has been developed and refined over years. Finally, after a few iterations, it is scalable and extremely powerful. Only the final system will be described in the following sections, although it was not yet available to its full extent for earlier tests.

The data acquisition and analysis software, which I entirely wrote on my own, was improved together with the hardware. While it originally was a simple text-based program confined to a special hardware, it has evolved to a fully configurable DAQ system with advanced online analysis and a graphical user interface (GUI). Only the cooperation of hardware and software features reveals the full power of such a test system.

### 5.1.1 Hardware Setup

The APV setup at HEPHY fulfills a functionality similar to the final CMS readout system, but it is smaller and in several aspects easier to handle. Fig. 5.1 shows the building blocks of our setup for the readout of a single APV hybrid without an attached detector.

This configuration is typically used in a laboratory for testing chips or hybrids and their properties. The APV hybrid is connected to a repeater board, which buffers the signals and provides local voltage regulators. It is connected to three VME boards: the APV sequencer, which basically delivers clock and trigger signals, the VME-$I^2C$, which hosts an $I^2C$ bus master, and a multi-channel VME-ADC. The configuration shown here has four analog channels, thus it can read out up to four APVs directly or up to eight APVs when using the APVMUX, which

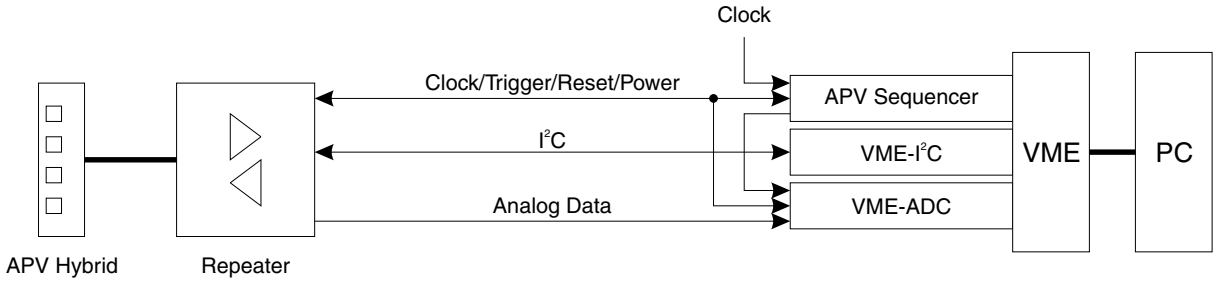



Figure 5.1: Schematic view of the simple APV setup at HEPHY.

combines the output of APV pairs onto one analog line (see section 4.2.1, p. 63). A commercial VME bus controller provides an interface to the PC, which controls the modules and reads back data.

The APV25 hybrid, repeater and the VME modules were designed and built at HEPHY. These home-made components of the APV setup will be discussed in the following sections.

#### 5.1.1.1 APV Hybrid and Repeater

One or more APV chips are mounted on a hybrid together with decoupling capacitors and termination resistors. Since the chips are glued and bonded, the APV footing has to match the chip version. Two different APV25 hybrids were developed at HEPHY. Fig. 5.2 shows the APV25S0 hybrid for up to four chips, while the other hybrid (fig. 5.30, p. 100) was specifically designed for the APV25S1 irradiation test.

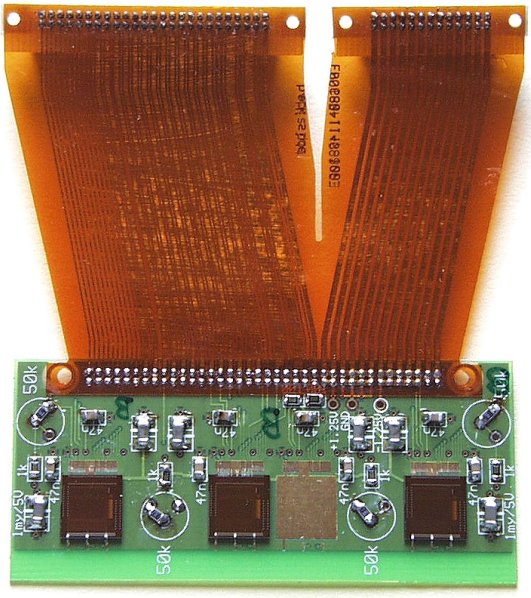


Figure 5.2: A Vienna APV25S0 hybrid equipped with three chips.

The schematic diagram of the repeater is shown in fig. 5.3. Local voltage regulators provide the power to the APVs, while reset, clock and trigger signals are buffered and sent to the APV hybrid. Optionally, when using the APVMUX which includes a PLL, clock and trigger are

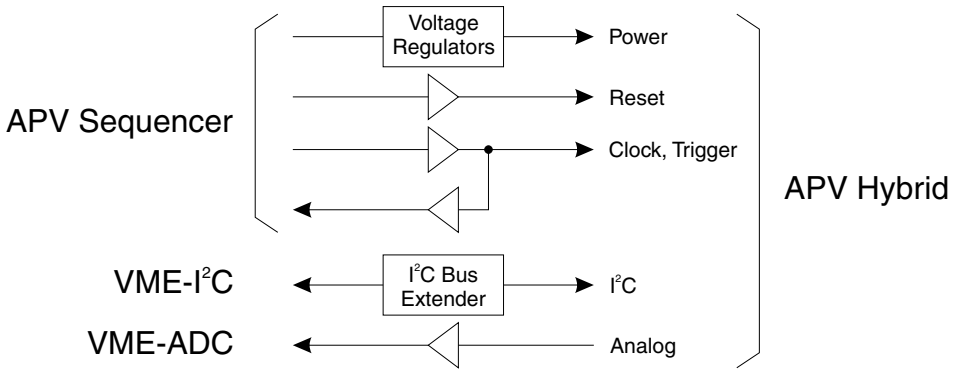



Figure 5.3: Block diagram of the HEPHY repeater.

combined into a single signal. Moreover, clock and trigger signals are also sent back to the VME system. The returning clock has a constant delay with respect to the APV clock and does not depend on delay adjustments made in the APV sequencer. Thus, it is perfectly useful for the digitization.

The $I^2C$ bus of the APV hybrid is buffered with an extender and the levels are adapted to those of the APV supply. Four fast amplifiers deliver the analog output of the APVs to the VME-ADC. Once, a silicon detector module with eight APV6 chips was read out using the analog stage of a second repeater in parallel.

Since the power supply voltages, the output stages and other details differ between APV6 and APV25 versions two different repeater boards were developed for their readout.

#### 5.1.1.2 APV Sequencer

The APV sequencer (fig. 5.4) is the core of the HEPHY setup.

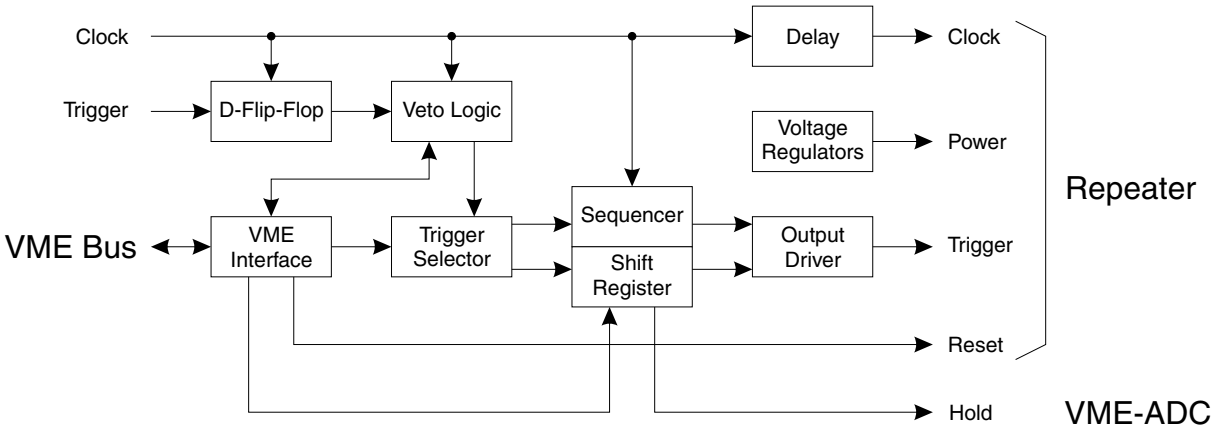



Figure 5.4: Block diagram of the HEPHY APV sequencer.

The module is driven by an external clock source (usually 40 MHz). Triggers are either derived from an input on the front panel ("hardware triggers") or generated by a VME command ("software triggers"). The hardware triggers have to pass through a D-Flip-Flop to synchronize with the clock. There, incoming triggers are only accepted if they are at logically high level

during the clock edge. Synchronized triggers are then sent through a programmable veto logic which can block them. By default, the veto logic allows only a single trigger until its state is cleared by VME. However, the number of allowed trigger pulses can be set between one and eight. The veto state can also be set by a VME command to disable hardware triggers at all. Moreover, the veto logic ensures that the minimum distance between subsequent triggers is three clock cycles. Otherwise, the pattern would be interpreted as a special symbol (see tab. 4.1, p. 51).

The effect of hardware triggers which have passed the veto logic or software triggers depends on the mode of operation. Either the trigger is delayed in a shift register or a programmable bit pattern is taken from an internal memory. In the first case, a digital pipeline of programmable length is used to delay the trigger sequence arriving at its input. Several triggers can be allowed to pass through the veto logic, consequently being delayed and streamed to the APV. This feature is useful to study the effect of frequent particle triggers. The second mode is mainly used for sending special symbols on the trigger line. Four different sequences of 256 bits are stored in an internal memory. One of them or several in parallel can be activated by a software or hardware trigger. By default, the four sequences are loaded with soft reset (101), calibration (110...011), a software and a hardware trigger (000...010...) at different positions. To send an APV reset, the 101 sequence is issued by software. For internal calibration, the 11-memory together with a software trigger is activated and the calibration request is followed by another 11-pattern to dump the calibration pulse of opposite polarity (see section 4.1.1.5, p. 59). The sequencer can also be used to generate a series of subsequent APV triggers initiated by a single hardware trigger. With the APV25 in multi-peak mode, this feature allows to effectively get a sequence of samples separated only by a single clock cycle. This powerful feature will be presented together with measurements in more detail in section 5.1.5.4, p. 97.

A trigger sequence can signal the VME-ADC to start a conversion sequence but may not necessarily do so. In fact, such a "hold" signal is issued except when only the soft reset or pure calibration requests are activated, since neither of these produce any APV output. The calibration pulse is only seen in conjunction with a software trigger, which also generates a hold signal for the ADC.

Voltage regulators provide the power for an attached repeater board. The clock which is sent to the repeater can be delayed to match the phase of the trigger signals and finally, a hard reset signal for the APV can be generated by a VME command. For test purposes, the trigger propagation can be switched to transparent mode, where the whole processing is bypassed and the input is directly sent to the repeater.

#### 5.1.1.3 VME-$I^2C$

An interface between VME and $I^2C$ buses is provided by the VME-$I^2C$ board. As seen in the block diagram (fig. 5.5), the functionality of this module is straight-forward. The VME bus is bridged to an $I^2C$ bus master, followed by an opto-coupler and a bus extender.

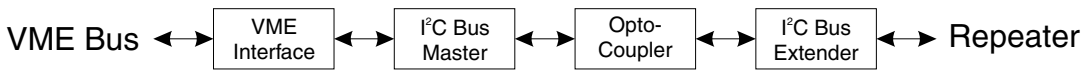



Figure 5.5: Block diagram of the HEPHY VME-$I^2C$.

An opto-coupler is used to connect $I^2C$ signals of different voltage levels. This implies that the bus extender is powered by the remote repeater. Originally, the $I^2C$ bus was intended

for communication between components on a single board and thus has a limited line drive capability. Between a set of two extenders, the line currents are amplified to cope with the higher capacitive load and noise.

#### 5.1.1.4 VME-ADC

The VME-ADC (fig. 5.6) is used to digitize the analog data coming from the APVs. Four input channels are amplified in the input stage and digitized by individual 12 bit ADCs with the input clock frequency (normally 40 MHz). When a hold signal is asserted, up to 4096 samples are stored in FIFOs, which can be read over the VME bus.

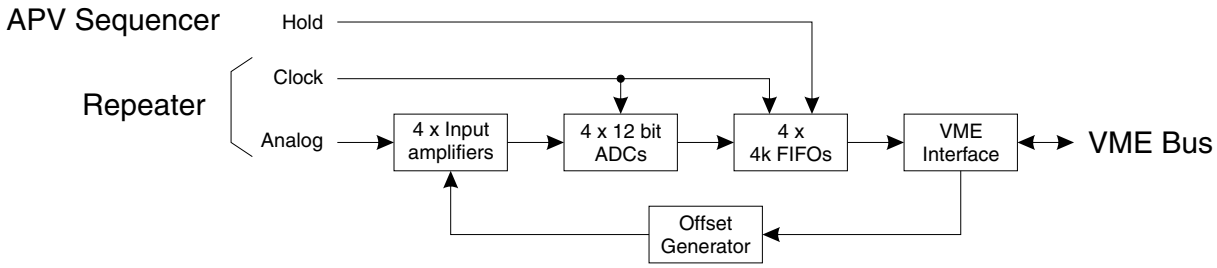



Figure 5.6: Block diagram of the HEPHY VME-ADC.

The differential input range of the VME-ADC is ±750 mV. Although never used, also half of this range can be selected. An individually programmable offset is added to each channel in the input stage. Thus, the input range can be shifted by approximately ±300 mV. A −3 dB bandwidth of 50 MHz has been measured for the analog inputs, which is mainly determined by one particular input amplifier. A considerably higher bandwidth has been achieved when omitting this amplifier at the price of less gain. This modification was only done for the APVMUX test (see section 5.1.7, p. 107), since its output is clocked with 40 MHz compared to 20 MHz with a non-multiplexed APV. In the latter case, two samples are obtained for each APV channel data. For optimum digitization, the clock timing was optimized for the second sample, while discarding the first point which is spoiled by transients.

#### 5.1.1.5 Module Test Setup

The same APV setup is also used for module tests with source or beam operation. In that case, several APV hybrids are read out in parallel. Thus, additional components for power and signal distribution are required as well as HV supplies for the detector bias.

Fig. 5.7 shows the extended setup for four detector modules. The front-end electronics to the left is located in the beam area, while the right half is located in the control room. The maximum cable length already tested between these parts was 25 m.

Several silicon detector modules are placed in a particle beam. Each module needs its own repeater board, which can be either the HEPHY repeater discussed in section 5.1.1.1, p. 73, or the Perugia TRI card, which has similar functionality. Different APV versions can be mixed provided that each APV is equipped with the appropriate repeater type. A front-end distribution board delivers power and signals to each repeater.

The particle trigger is derived from a scintillator watched by two photomultiplier (PM) tubes. The trigger signals from the PMs are processed by standard NIM (Nuclear Instrumentation

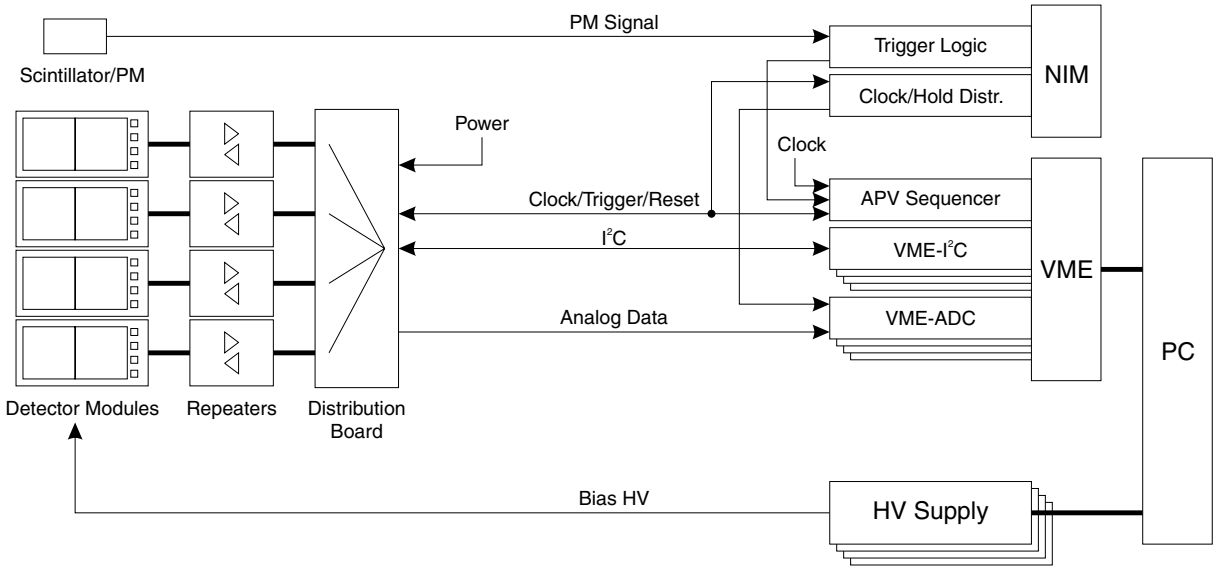



Figure 5.7: Schematic view of the HEPHY module test setup.

Module) logic modules. After two independent discriminators, the coincidence of the two PMs is formed and sent into an adjustable delay. Its output is shaped to a short pulse of 5 ns duration and fed into the APV sequencer in the VME crate. As the sequencer input is equipped with a D-Flip-Flop, only triggers within a small window with respect to the clock edge are accepted. This feature effectively synchronizes the beam with the APV clock.

Individual VME-$I^2C$ and VME-ADC modules are intended for each detector module. The clock returned by one of the repeaters is sent into a clock and hold distribution board, which combines these signals in such a way that there is only a clock when the hold line is asserted. The combined clock/hold can be delayed in three individual groups before being distributed to the VME-ADC modules. Thus, the clock timing can be adjusted for each ADC. Experiments have shown that the timing needs to be adjusted for different types of repeater boards and in particular between APV6 and APV25 chips. Naturally, analog signals from different modules can be sent into the same VME-ADC board if the timing is compatible. Moreover, several modules can be connected to the same $I^2C$ bus if all APV chip addresses are unique.

#### 5.1.1.6 Cooling Box

A cooling box for up to seven detector modules was developed at HEPHY [60] to provide conditions as close as possible to the CMS tracker. An ambient temperature of $-10°$ C is even mandatory when testing irradiated sensors (see section 2.3.2, p. 26). The cooling box is based on direct-to-liquid cooling elements employing the thermoelectric effect discovered by J.C.A.Peltier[1]. This principle was soon adopted by the CMS collaboration for other test setups after successful operation in our beam tests.

Two highly efficient Peltier elements with an electrical power consumption of up to 350 W each are used to cool the interior of an isolated box. The heat at the warm side of the elements

[1] Jean-Charles-Athanase Peltier, *1785 in Ham (France), †1845 in Paris. In 1834 the French physicist discovered that at the junction of two dissimilar metals an electric current will produce heat or cold, depending on the direction of the current flow. Later he introduced the concept of electrostatic induction.

is carried away by water flow. This method outperforms air cooling, because the Peltier performance degrades with the temperature difference between warm and cold sides. While the warm side is tied to the tap water temperature, which is usually between 10 and 20° C, air cooling would inevitably cause a warm side considerably above room temperature.

The cold side of the Peltier elements is connected to two massive aluminum plates at top and bottom ends inside the box. Small aluminum boxes, which carry the silicon detector modules, are inserted into rails in the aluminum plates. Thus, the small boxes are thermally connected to the Peltier elements. To prevent condensation of water on sensitive elements, the cooling box is flushed with a dry gas (e.g. nitrogen) prior to and during cooling. Inside the cooling box, the gas is first guided through caverns in the aluminum plates to cool it down. Then, it flushes the small boxes and exhausts into the large volume.

Not only the mechanics, but also the power supplies for the Peltier elements and their control and readout interface have been developed at HEPHY. Moreover, a ten-channel temperature monitoring system (MultiTherm) was built to watch the system temperature in several spots and automatically control the power supplies of the Peltier elements for a set temperature.

In terms of control theory, the conversion of electric power at the Peltier elements to the temperature decrease inside the box reveals $PT_1$ behavior with a short dead time. At typical internal heat dissipation, a time constant of approximately 45 min and a dead time of about 10 min were measured.

### 5.1.2 Software

#### 5.1.2.1 DAQ and Analysis Software

The data acquisition (DAQ) software is used to interactively control the APV setup hardware and read out the analog data, which are written to disk. Moreover, it provides an online analysis for monitoring purposes. The offline analysis software, using a refined code with additional features, reads the data from disk and performs an extended evaluation.

Both versions of the APV software run in the LabWindows/CVI environment by National Instruments on a PC under Windows NT. While providing the same graphical user interface (GUI) features as the wide-spread LabView package, the CVI software is entirely written in the C programming language.

The data are not acquired continuously for lack of disk space, but in single runs with a defined set of parameters and conditions. Such a run consists of an initialization phase with pedestal and noise evaluation followed by the main part of data acquisition.

Depending on the intention of the operator, various run types are possible in the HEPHY APV readout system:

- Hardware (normal particle triggers)
- Hardware Scan (series of hardware runs with a delay scan)
- Software (pedestal run)
- Internal Calibration Scan
- External Calibration Scan

A normal run with hardware triggers is used for source or beam operation. The hardware scan is intended for optimization of timing parameters. In this case, an external VME-controlled

delay is stepped through a defined range and hardware runs are performed for each step. When the delay is e.g. inserted in the ADC clock line, the optimum conversion point can be found. A software triggered run does not need any external trigger input and thus is good for test purposes and evaluation of the system noise. Calibration Scans are used for the composition of a continuous APV output waveform as if the data were not sampled. This can be achieved using either the internal calibration circuit or an external voltage step applied to an APV input over a capacitor. With such a calibration scan, the shaper output can easily be compared to the output after deconvolution. Moreover, the effect of preamplifier and shaper bias currents can be studied.

Each run follows a certain sequence:

- Hardware initialization
  - VME boards initialization
  - APV reset
  - APV register programming
- Software initialization
  - 200 events pedestal evaluation
  - 200 events noise evaluation (pass 1)
  - 200 events noise evaluation (pass 2)
- N events according to run type

Initially, the VME boards are reset and initialized, followed by hard and soft resets are applied to the APVs and register programming. After the hardware is set to a defined state, 600 events with software triggers are taken regardless of the run type, which are used for pedestal and noise evaluation. These values must be known for each single channel to be able to properly extract particle hits or calibration signals from subsequent data.

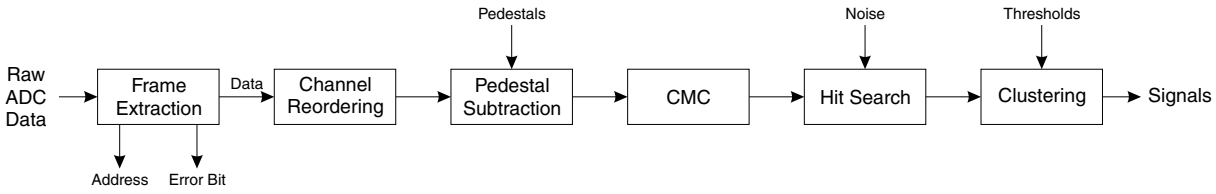



Figure 5.8: Event processing from the raw ADC data to extracted signals.

Fig. 5.8 illustrates the calculations performed on a single event. The input of the event processing algorithm are the raw ADC data. The APV output frame(s) must be extracted from this data stream, returning the pipeline address, the error bit and the channel data. Due to the APV output multiplexer, the channel output order does not correspond to the physical order (see section 4.1.1.4, p. 57) and thus must be reordered.

Then, the pedestal (zero input) values are subtracted for each channel, which is also known as zero-suppression. Low-frequency noise such as an AC line ripple results in DC shifts of all data within an APV frame. This shift is removed by the common-mode correction (CMC),

which basically calculates an average of all channels, which is then subtracted from each channel. Channels which may contain signals must be skipped in the averaging process. Pedestal subtraction and CMC can be performed in reverse order as well, but the shown sequence is more illustrative. The output after these steps is essentially zero in all channels except those containing a signal. However, due to the intrinsic noise of the amplifier it is only a flat line in statistical average.

The extraction of signals is usually done with a threshold in terms of RMS noise. A hit is recognized when a channel exceeds a certain signal-to-noise ratio. To account for particle hits with signals shared by adjacent channels, the signals of neighboring channels are added as long as they also exceed a threshold. This procedure is known as clustering and the number of strips signaling a single particle is called cluster width. It is common to define three thresholds for the clustering algorithm: a seed strip cut, a cut for neighboring strips and finally a total cluster cut. All these thresholds are expressed in terms of the RMS noise of the corresponding channels.

In our analysis, we normally use $6/3/6\,\sigma$, when $\sigma$ denotes the noise. In this case, the total cluster cut is meaningless since it is already fulfilled by the seed strip alone. The cuts used by the official CMS analysis are slightly lower: $3/2/5\,\sigma$. For the beam test data on prototype modules, we found that these values cause a considerable number of fake hits with some modules and therefore generally used higher cuts.

The output signals are converted to charge units using either internal or external calibration data. Alternatively, the signal-to-noise distribution can be generated which is basically proportional to the signal but needs no calibration. When operating with a $^{90}$Sr $\beta$ source or a beam delivering approximately minimum ionizing particles (MIPs), the resulting signal (or SNR) distribution is fitted by a Landau-Gauss convolute (see section 2.1, p. 14) with a separate application embedded in the ROOT analysis package [61]. At lower particle energies, a simple Gauss fit is applied to the signal (or SNR) distribution. Examples of such Landau-like and Gauss-like signal distributions are shown in fig. 5.20, p. 91.

Moreover, a hit map distribution can be obtained when the signal positions are filled into a histogram. The correlation of particle hits in several planes can be used to apply further cuts to the signals. This feature, which is not included in the HEPHY software, is known as tracking. As discussed in section 1.3, p. 11, this track reconstruction will be an essential tool for charge and momentum identification of particles traversing the magnetic field of the CMS Silicon Strip Tracker.

For the initial pedestal calculation, only frame extraction and data reordering are performed. During the noise evaluation, the event processing is stopped after pedestal subtraction and CMC. A second pass of the noise evaluation is done for a refined analysis, where accidental particle hits which can happen in a high intensity beam even with random triggers, are excluded from CMC and noise calculation. In other analysis algorithms, pedestal and noise values are constantly updated throughout the run to account for slow drifts. However, this was not necessary in our case with a typical run time of only five minutes and thus not included in the software.

Fig. 5.9 shows a screenshot of the data acquisition software. The displayed waveform is the raw ADC output of an APV25S1 with an external calibration signal applied to four channels.

The most important settings of the APV DAQ software are made on the GUI. Many other adjustment values are written into a configuration file, which is read by the program at startup. Thus, the system is scalable and very flexible, yet still easy to handle for the normal user.

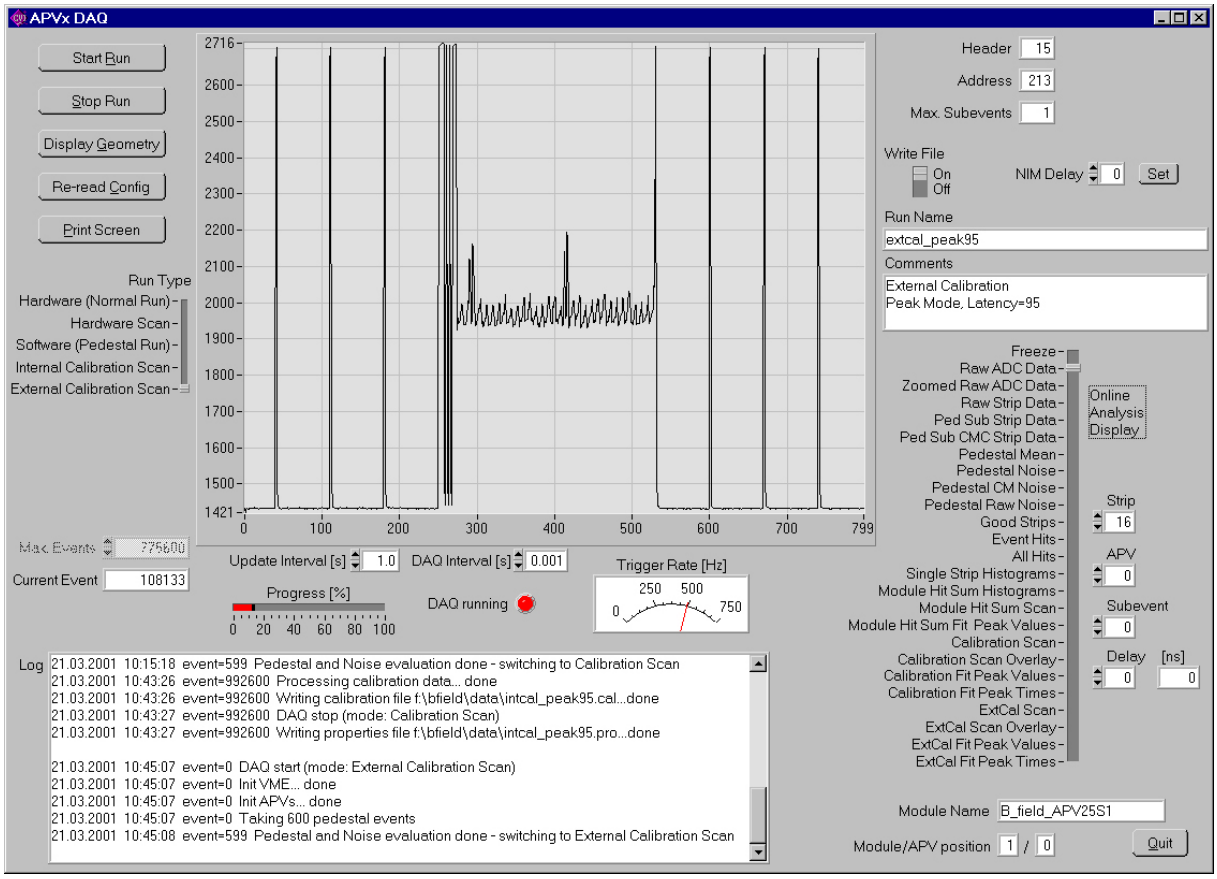



Figure 5.9: Screenshot of the APV data acquisition software.

#### 5.1.2.2 Slow Control Software

A second PC is used for tasks typically known as "slow control". This includes the control and monitoring of the cooling box as well as monitoring of the detector leakage currents.

The slow control software periodically reads the temperature measured by the connected probes and compares the set value to the actual temperature in a specified location. A PI controller algorithm is used to adjust the power such that the system follows the desired temperature. Moreover, the voltages and currents for the detector bias are monitored continuously. All data are logged to disk and compared with individual limits. An alarm condition is set when one or more limits are exceeded, which optionally generates an email or SMS notification.

A screenshot of the slow control software is shown in fig. 5.10, displaying the temperature and cooling power history during a test of the cooling box. Only a single power supply (with zero output) was connected at that time.

### 5.1.3 APV6 Multiregion Module Beam Test (June 1998)

The very first silicon detector module with APV6 readout was constructed in early 1998 at HEPHY. Three chips were amplifying the signals of a single silicon detector with 384 strips. The assembled detector module was tested both in laboratory with a source and in a particle beam at CERN. Detailed information about the setup can be obtained at [62].

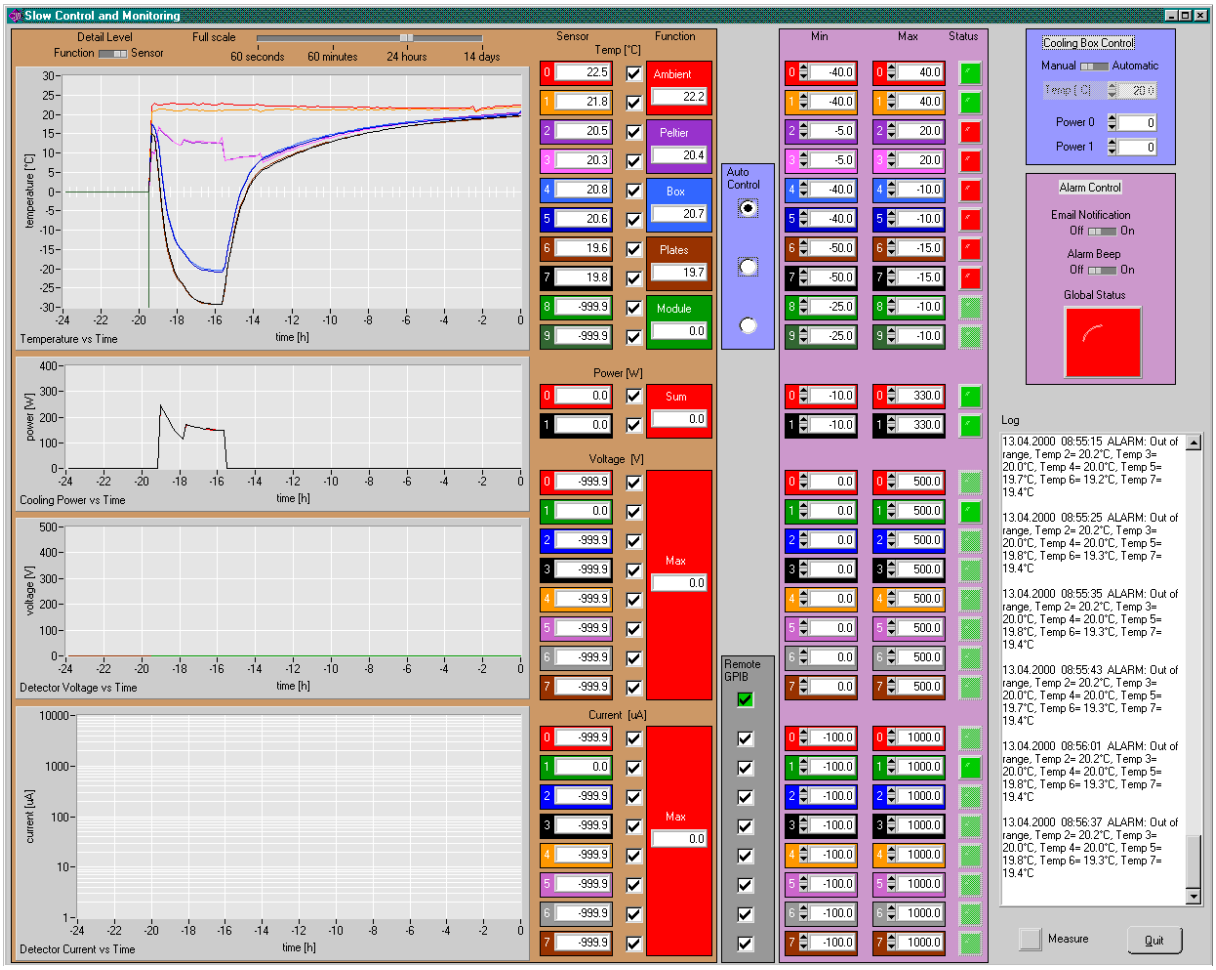



Figure 5.10: Screenshot of the slow control software.

Fig. 5.11 shows this silicon detector module on a support together with an early repeater and temperature probes. The multiregion detector had twelve domains of 32 strips each with varying geometry specified in tab. 5.1. Each zone was surrounded by a guard ring structure, as shown in the detailed view of fig. 5.12.

| **Zone** | **0** | **1** | **2** | **3** | **4** | **5** | **6** | **7** | **8** | **9** | **10** | **11** |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Strip pitch** [$\mu$m] | 60 | 80 | 240 | 120 | 60 | 80 | 240 | 120 | 60 | 80 | 240 | 120 |
| **Implant width** [$\mu$m] | 25 | 40 | 70 | 50 | 20 | 25 | 50 | 35 | 15 | 15 | 30 | 20 |

Table 5.1: Strip pitch and implant width values of the multiregion silicon detector.

The beam data were already analyzed and published [62] shortly after the beam test. However, to get consistent results with later beam tests, the raw data were completely re-analyzed with the same software and parameters that were used for the other tests. Thus, the results presented here are slightly different from what was published earlier, but allow direct comparison to the other APV measurements.

The beam test was performed at the X5 beamline of the SPS accelerator at CERN. It

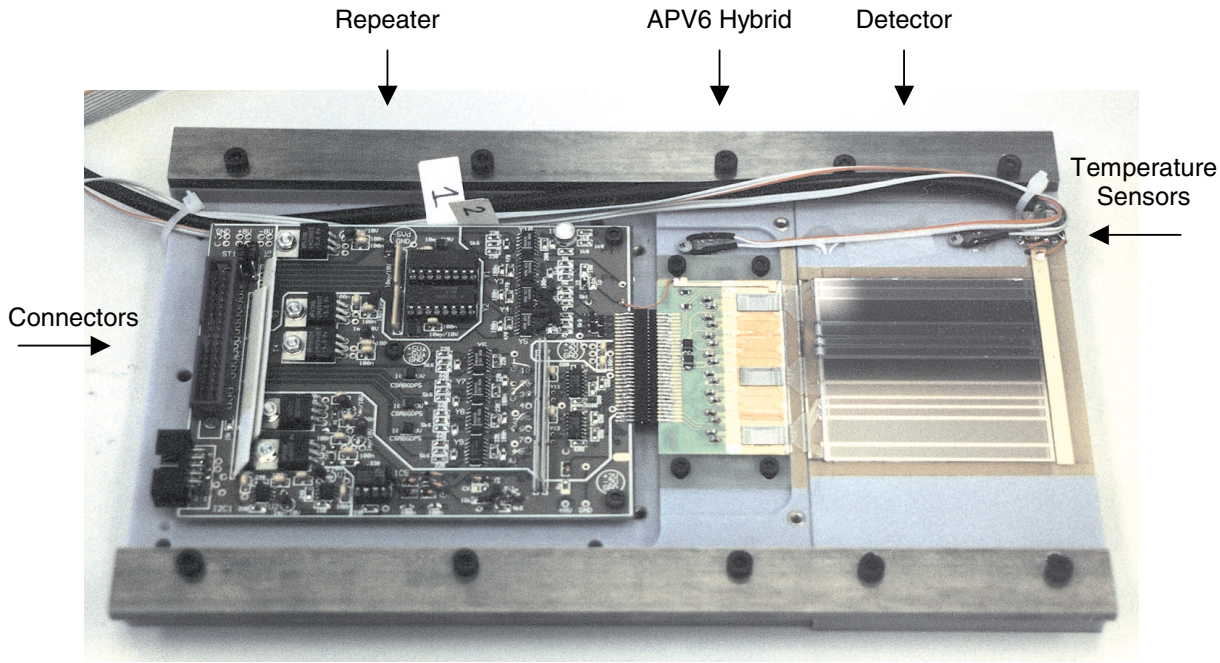



Figure 5.11: The first silicon detector module with APV6 readout.

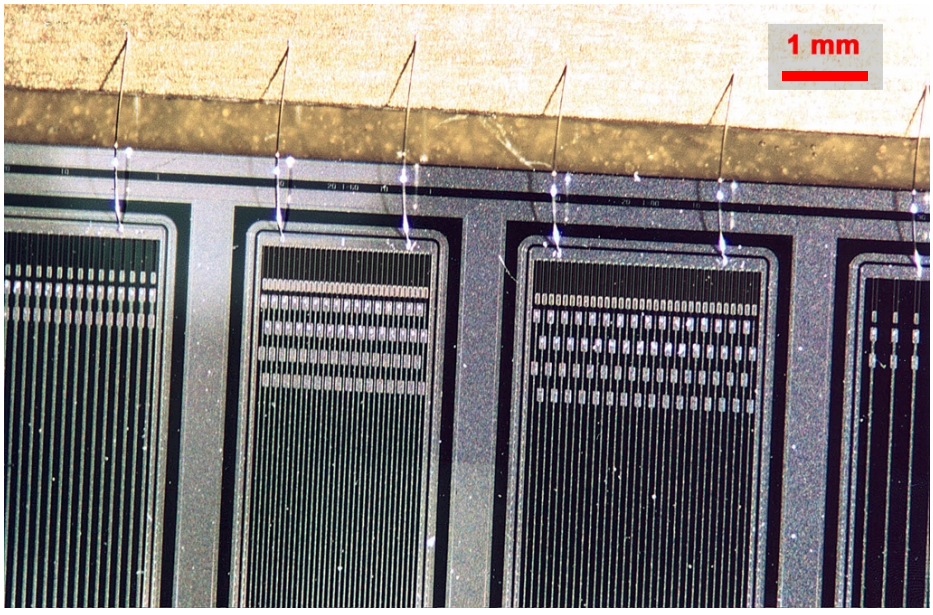



Figure 5.12: Detail of the multiregion detector showing the guard rings surrounding each zone. The bond wires on top connect the polysilicon resistors to the HV rail.

delivers highly relativistic pions and muons with a momentum of 100 GeV/c, which have a mean ionization of 6% above the MIP level. This excess is approximately compensated by a small jitter of the trigger relative to the particle crossing. The module was placed in a moderately cooled environment at an ambient temperature of 14° C, where all measurements were performed in deconvolution mode.

According to eq. 2.29, p. 30, the strip capacitance is a linear function of $w/p$. Moreover, the amplifier noise, as shown in eq. 2.35, p. 36, linearly depends on the capacitance and thus on $w/p$. The SNR implicitly takes over the inverse functional dependence as shown in fig. 5.13. The prediction has been obtained from capacitance values calculated by eq. 2.29, an APV6 amplifier noise of 1125 e + 65 e/pF and a MIP charge of 25000 e.

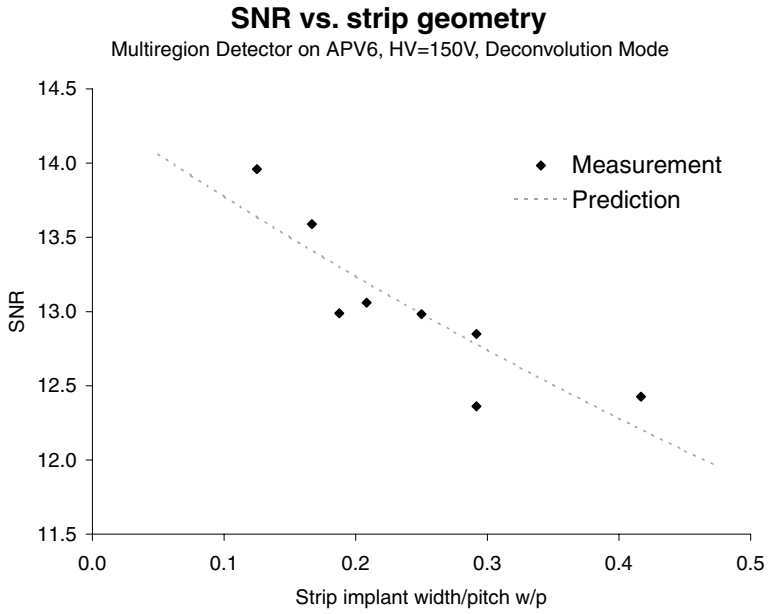



Figure 5.13: SNR vs. strip geometry of the multiregion detector.

These results were measured at a bias voltage of 150 V. Other runs were performed at 100 V, resulting in SNR values between 10.6 and 12.7, depending on the zone. The SNR decrease of approximately 10% indicates that the multiregion detector was not fully depleted at 100 V.

An angle scan between 0° and 30° was performed on two different zones. Due to the longer path of particles in the detector, the deposited energy and thus the signal increases. In relation to the collected charge $Q_0$ at perpendicular incidence (0°), the charge $Q_\alpha$ at a tilt angle $\alpha$ is given by

$$\frac{Q_\alpha}{Q_0} = \frac{1}{\cos\alpha} \quad . \tag{5.1}$$

Moreover, the cluster width increases with the tilt angle. In this case, pure geometry does not fit the experimental results, since the average cluster width is slightly above one already at 0°. An empirical approach, which was successfully applied to a large number of angle scans [63], leads to

$$\mathrm{clw} \propto \sqrt{\tan^2\alpha + \mathrm{const}^2} \quad , \tag{5.2}$$

where clw is the average cluster width and const a fit parameter.

Fig. 5.14 shows the dependence of the cluster width on the tilt angle for two different zones with the fit function (eq. 5.2) applied. Due to geometrical reasons, the projection of an inclined particle track covers a larger number of strips if their pitch is smaller, explaining the different cluster width curves.

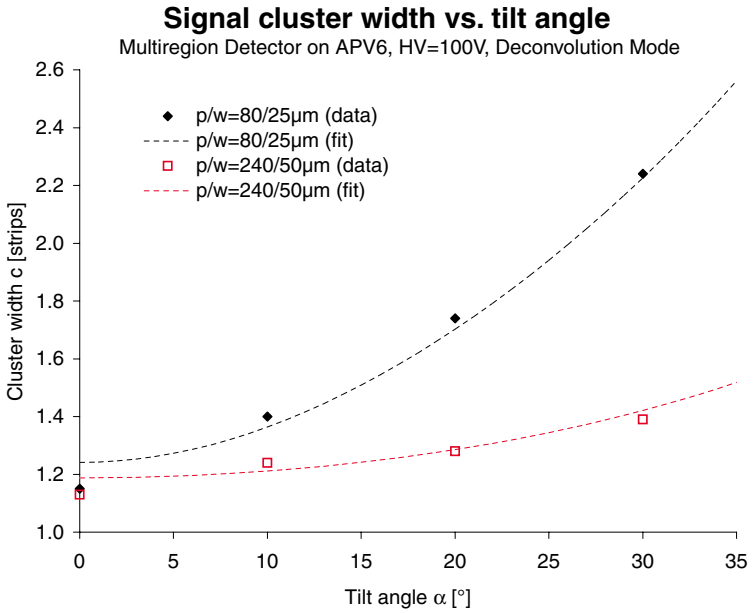



Figure 5.14: The cluster width increases with the tilt angle with a slope depending on the strip pitch.

After the beam test, source tests were performed with the same setup, yielding compatible results.

### 5.1.4 APV25 Laboratory Tests (2000/2001)

#### 5.1.4.1 Calibration and Noise

Precise calibration measurements were performed on the APV25S1, which was mounted on a single-chip hybrid (fig. 5.30, p. 100). Small capacitors are integrated in the PCB (printed circuit board) hybrid to allow pulsing by an applied voltage step. The placement of such capacitors with an associated voltage divider is difficult in terms of precision and excess noise introduced to the corresponding channels.

Pulse scans were performed for both internal and external calibration. The results with a nominal charge injection of 1 MIP (22500 e) are shown in fig. 5.15 for both peak and deconvolution modes. The waveform with external pulsing is not perfectly straight due to limited precision of the external delay used for this scan. While the shapes for internal and external calibration are congruent, their amplitudes differ considerably. The precision of the internal calibration circuit is limited for reasons discussed in section 4.1.1.5, p. 59. For this particular sample, the internal calibration charge is about 40% higher than the externally applied charge with an estimated accuracy of ±20%.

With a known calibration amplitude, the APV noise can be obtained in absolute numbers. We will use the external calibration for this evaluation, since it is the worse case in terms of absolute noise. Thus, the resulting numbers rather give an upper limit for the noise figure.

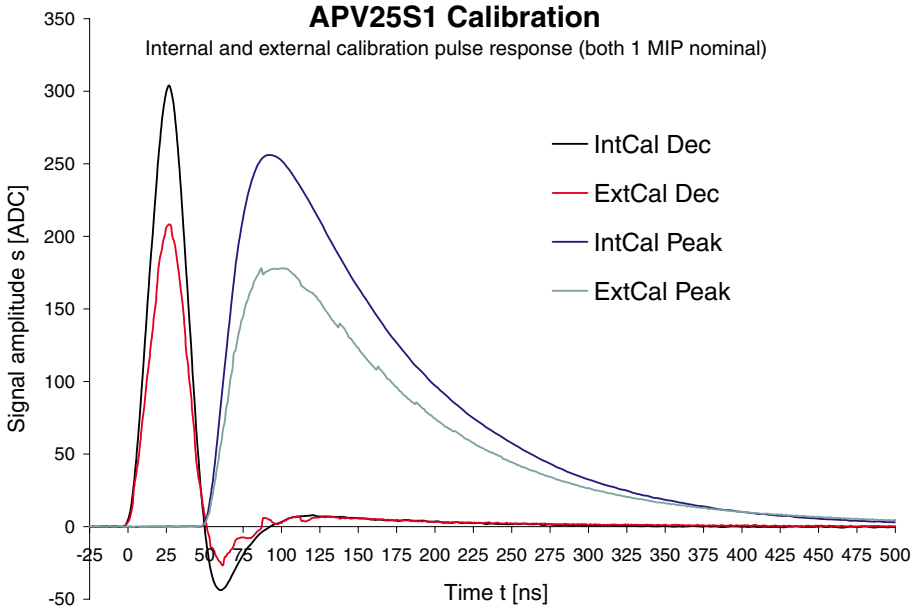



Figure 5.15: Comparison of the APV25S1 response to internal and external calibration pulsing for both peak and deconvolution modes.

After subtracting the noise of the readout system, the resulting equivalent noise charge (ENC) for channels with no capacitive load is shown in tab. 5.2. These numbers perfectly agree with the design values and with manufacturer's tests [64].

| **Mode** | **Design** ENC [e] | **Measurement** ENC [e] |
|---|---|---|
| Peak | 250 | 267 |
| Deconvolution | 400 | 425 |

Table 5.2: Comparison of the APV25S1 equivalent noise charge design values to measurements with external calibration. The noise of the readout system has been subtracted.

#### 5.1.4.2 Source Test

The first silicon detector module ever with APV25 readout was assembled in early 2000 at HEPHY. It is made of two silicon detectors from 6" wafers, which are partially read out by three APV25S0 chips. The detector thickness is 320 $\mu$m with a strip pitch of 140 $\mu$m. This "Vienna APV25" (V25) module is shown in fig. 5.16.

A module test with a collimated $^{90}$Sr source was performed in peak and deconvolution modes. In both cases, the signal is approximately Landau-distributed as shown in fig. 5.17.

Unfortunately, one of the attached sensors showed current fluctuations at room temperature resulting in excess noise. In a beam test, this module was operated at $-10^{\circ}$ C, where the current was stable up to approximately twice the depletion voltage, and reasonable SNR numbers will be stated in that context (following section).

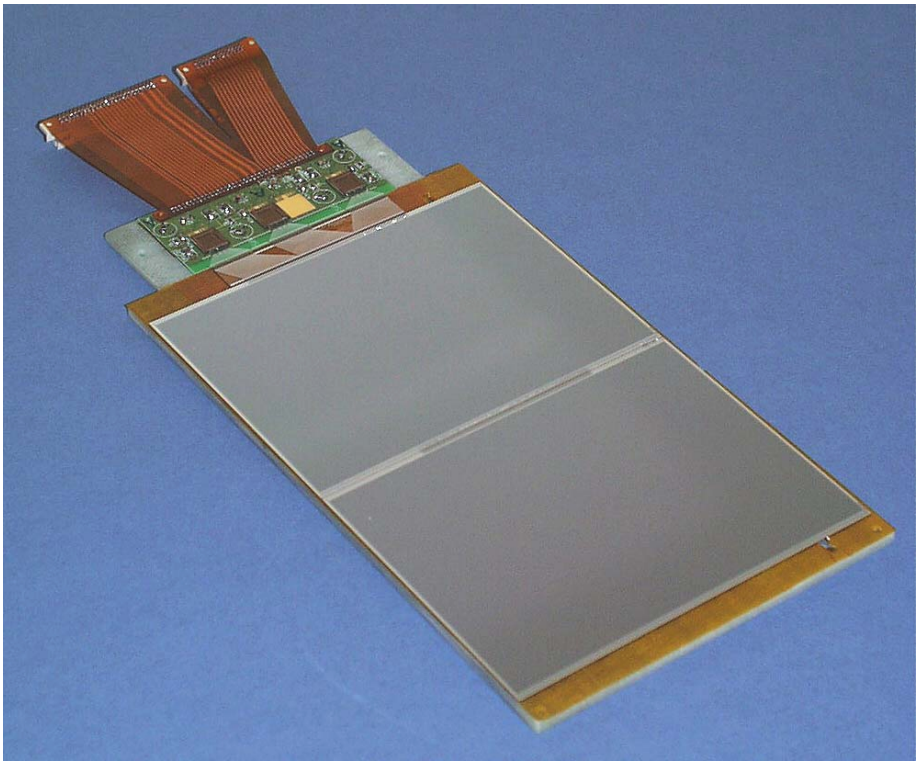


Figure 5.16: The Vienna APV25 silicon detector module.

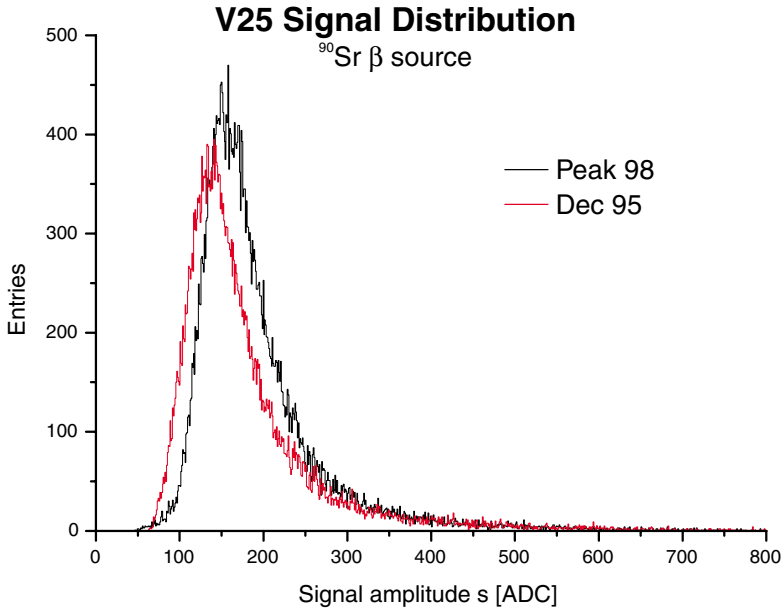



Figure 5.17: Signal distribution of the V25 module with a source test in peak and deconvolution modes.

### 5.1.5 APV6/APV25 Beam Tests (May/December 2000)

In May and December 2000, several silicon detector modules with APV6 and APV25 readout were tested in a PSI [65] particle beam. At PSI, a proton beam of approximately 1.7 mA is accelerated in a cyclotron driven by a 0.8 MW oscillator at 50 MHz. The protons are guided to two targets, from which several secondary beamlines are forked. The particle momentum within these secondary lines is selected by bending magnets.

The beamline used in our tests was set to provide protons and positive pions at a momentum of 350 MeV/c. In most of the measurements, an aluminum plate was inserted upstream in the beamline which shields the protons but does not affect the pions. The focussing magnets were adjusted for a large beam spot of about $70 \times 70\,\mathrm{mm}^2$ FWHM.

#### 5.1.5.1 Setup

Unlike most other particle beams, PSI provides a continuous beam with an LHC-like bunch structure of 50 MHz. Since LHC and the APVs are only clocked with 40 MHz, a dedicated PLL-based NIM module has been developed, which derives a synchronous 40 MHz signal from the PSI clock. Moreover, this module produces a short SYNC pulse when both clocks are in phase, which occurs every 100 ns (fig. 5.18). The SYNC pulse is used to select particle triggers which are in phase with the APV clock. By this synchronization, four out of five possible triggers are discarded, but it is ensured that passing triggers are in phase with the APV clock. Thus, the system environment is very close to what it will be in CMS.

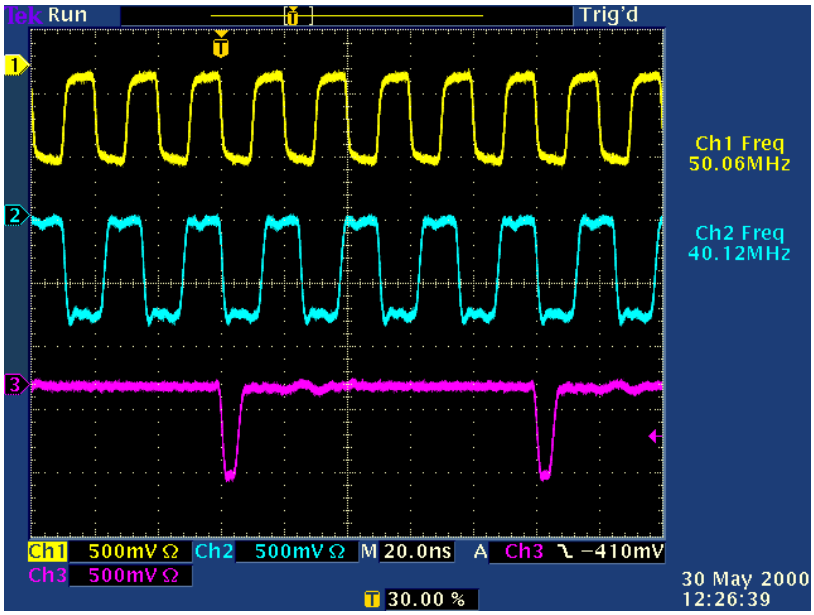



Figure 5.18: The synchronization module derives a 40 MHz clock (cyan) and SYNC pulses (purple) out of the 50 MHz PSI clock (yellow).

Normally, the beam was set to low intensity at the order of $10\,\mathrm{kHz\,cm}^{-2}$ with a particle trigger derived from a scintillator with an area of $12 \times 12\,\mathrm{mm}^2$, watched by two photomultiplier tubes. The photomultipliers were equipped with preamplifiers and operated at relatively low voltage to avoid saturation at high beam intensity. Several dedicated runs were taken at a

particle rate of up to 2.5 MHz cm$^{-2}$. At this intensity, it is not necessary to use the scintillator, because every bunch is filled with 2.5 particles in average. Thus, the SYNC pulse alone is good for triggering at high intensity. In that case, the measured beam profile is no longer restricted to the area covered by the scintillator, but reflects the actual beam spread.

Several silicon detector modules were tested at PSI, two of which were constructed at HEPHY. A module consisting of two 4" sensors with 1024 strips, read out by eight APV6 chips, was built within the framework of a module production milestone. Therefore, this module was called "Vienna Milestone" (VM). The "Vienna APV25" (V25; fig. 5.16, p. 87) module with two 6" sensors and APV25S0 readout was already presented in section 5.1.4.2, p. 86.

Several other institutes within the CMS collaboration joined these tests and provided their detector modules. In the May test, a total of five APV6 and two APV25S0 modules were tested, while in December, all six modules were read out with the new APV25S1 chip. Tab. 5.3 gives an overview of the properties for the modules tested at PSI. The module order corresponds to the arrangement in the beam as seen by the particles (from top to bottom).

| Date | Name | Built by | Sensors | Res. | Thickness [$\mu$m] | Pitch [$\mu$m] | Irradiated [cm$^{-2}$] | Readout |
|---|---|---|---|---|---|---|---|---|
| May 2000 | V25 | HEPHY | 2 × 6" | HR | 320 | 140 | no | 3 × APV25S0 |
| | KA1 | Karlsruhe | 1 × 6" | LR | 320 | 140 | no | 3 × APV6 |
| | PD1 | Padova | 2 × 4" | HR | 300 | 61 | no | 2 × APV6 |
| | PD3 | Padova | 2 × 4" | LR | 300 | 61 | no | 2 × APV6 |
| | PD4 | Padova | 2 × 4" | LR | 300 | 61 | $2 \cdot 10^{14}$ n | 2 × APV6 |
| | VM | HEPHY | 2 × 4" | HR | 300 | 61 | no | 8 × APV6 |
| | PD25 | Padova | 1 × 4" | LR | 300 | 61 | no | 1 × APV25S0 |
| December 2000 | BA1 | Bari | 2 × 4" | HR | 300 | 61 | no | 1 × APV25S1 |
| | KA2 | Karlsruhe | 2 × 4" | LR | 300 | 61 | $10^{14}$ p | 1 × APV25S1 |
| | PD27 | Padova | 2 × 4" | LR | 300 | 61 | $10^{14}$ p | 1 × APV25S1 |
| | BA2 | Bari | 2 × 4" | HR | 300 | 61 | $10^{14}$ p | 1 × APV25S1 |
| | PG | Perugia | 2 × 4" | LR | 300 | 61 | no | 1 × APV25S1 |
| | PD26 | Padova | 2 × 4" | LR | 300 | 61 | no | 1 × APV25S1 |

Table 5.3: Properties of the detector modules tested at PSI in May and December 2000. The silicon sensor resistivity is divided into low (LR, 1.4 ... 3.5 kΩ cm) and high (HR, 4 ... 8 kΩ cm) regimes.

Some of the silicon detectors were previously irradiated with CMS-like doses to study their performance in comparison with virgin sensors. This required an ambient temperature of −10° C, which was provided by the cooling box, shown in fig. 5.19.

The main results of the PSI module tests are presented in the following sections, while additional information is available at [12].

#### 5.1.5.2 Detector Module Performance

A few runs were dedicated to the comparison of energy loss between pions and protons at a momentum of 350 MeV/c. The pions are approximately minimum ionizing with a Landau-distributed energy loss, while the protons deposit much higher energy with almost Gaussian spread. Fig. 5.20 shows typical pion (left) and proton (right) signal distributions.

The measured energy loss is in good agreement with the restricted Bethe-Bloch theory (see section 2.1, p. 14), as shown in fig. 5.21. Since the pions are approximately minimum ionizing,

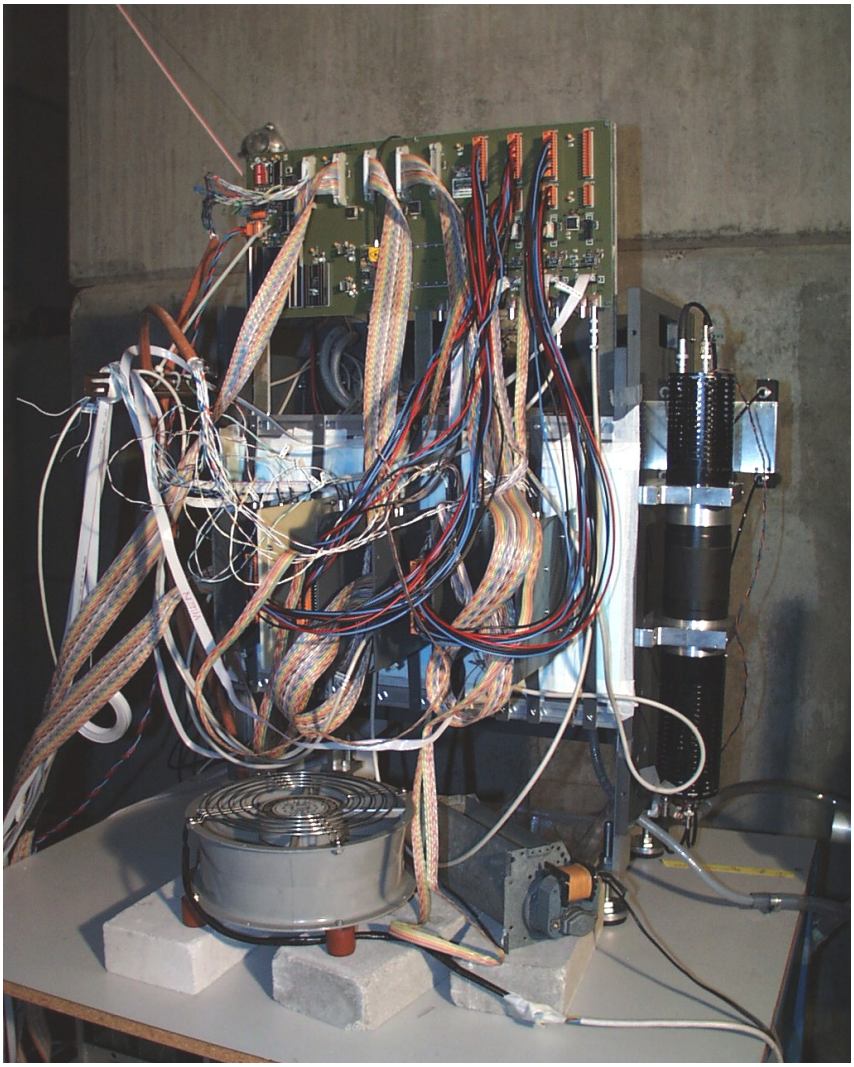


Figure 5.19: The fully equipped cooling box in the PSI beam area where the particle beam enters from the left. The rod to the right contain the trigger scintillator with two photomultipliers. The distribution board on the top of the box provides power, clock, trigger, reset and $I^2C$ signals to the repeater boards, which are located above the fan outside of the cooled environment, but connect to the detector modules inside.

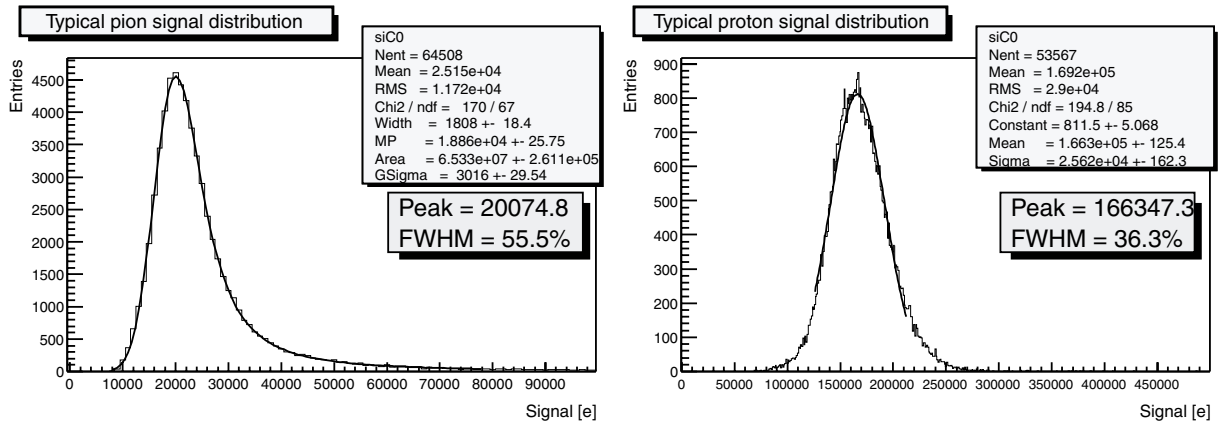



Figure 5.20: Typical pion (left) and proton (right) signal distributions measured at a momentum of 350 MeV/c. In the proton picture, the x axis range is five times larger in the pion plot. The absolute charge scale has been obtained from internal calibration, which is not very accurate.

they are the worst case in terms of the signal-to-noise ratio (SNR). Thus, all further results are obtained with pions except for the angle scan, where both pions and protons are compared.

The APV6 chip has a significantly higher noise contribution than its successor APV25. This reflects in the SNR values of the different modules. Fig. 5.22 shows the deconvolution mode SNR results of selected modules vs. the detector bias normalized to the respective non-irradiated depletion voltage. Several conclusions can be drawn from these curves. First of all, the APV25 readout outperforms the APV6. Tab. 5.4 shows typical SNR and the electronic noise values obtained with detector modules read out by APV6 and APV25 in peak and deconvolution modes.

| **Mode** | **APV6** | | **APV25** | |
|---|---|---|---|---|
| | ENC [e] | SNR | ENC [e] | SNR |
| Peak | 1400 | 16 | 900 | 25 |
| Deconvolution | 2250 | 10 | 1300 | 17 |

Table 5.4: Typical noise (ENC) and most probable signal-to-noise (SNR) values of full-size, non-irradiated CMS detector modules measured with minimum ionizing particles (MIPs).

With only one sensor, the capacitive load and thus the noise is lower, leading to a higher SNR as shown for the PD25 module in fig. 5.22 and for the multiregion detector in section 5.1.3, p. 81. Moreover, the SNR curves of irradiated silicon detectors need higher bias voltages and yet do not really saturate (see section 2.3.3, p. 28). Although the SNR of irradiated sensors is lower, their performance is still satisfactory for the application in the CMS tracker. From the detector simulation discussed in section 2.2, p. 17, a good approximation of the signal-to-noise ratio around and above depletion has been obtained.

Depending on the APV latency value, the sampled values are stored in the chip pipeline for a defined time. With variation of this latency between 25 and 150 clock cycles, no difference could be spotted in the signal-to-noise ratio. This demonstrates that the pipeline storage capacitors are able to hold their charges without noticeable leakage for at least 3.75 $\mu$s, exceeding the CMS first level trigger latency.

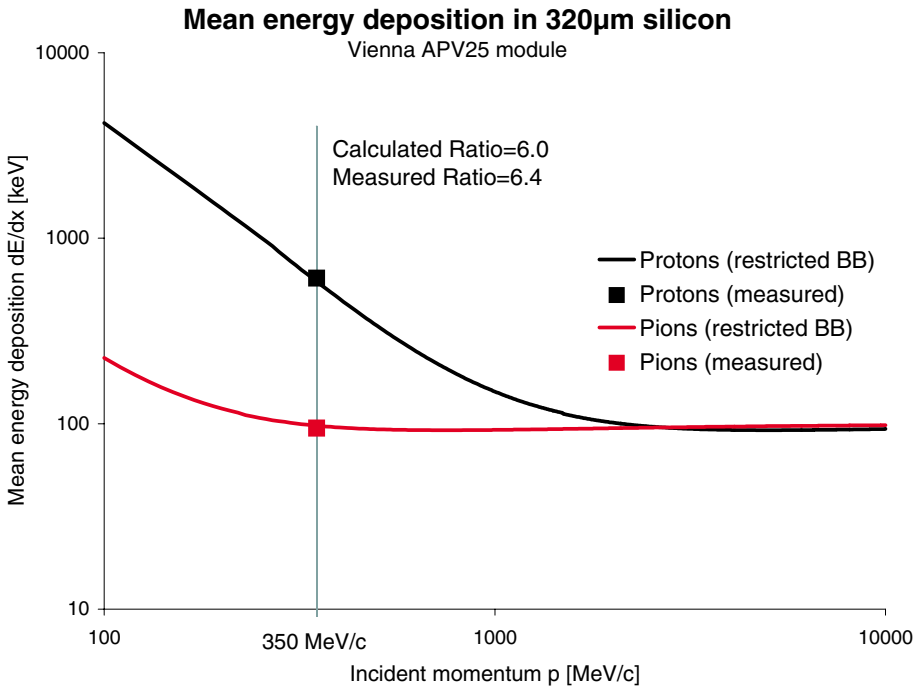



Figure 5.21: Measured energy loss of pions and protons in comparison to calculation from the restricted Bethe-Bloch theory.

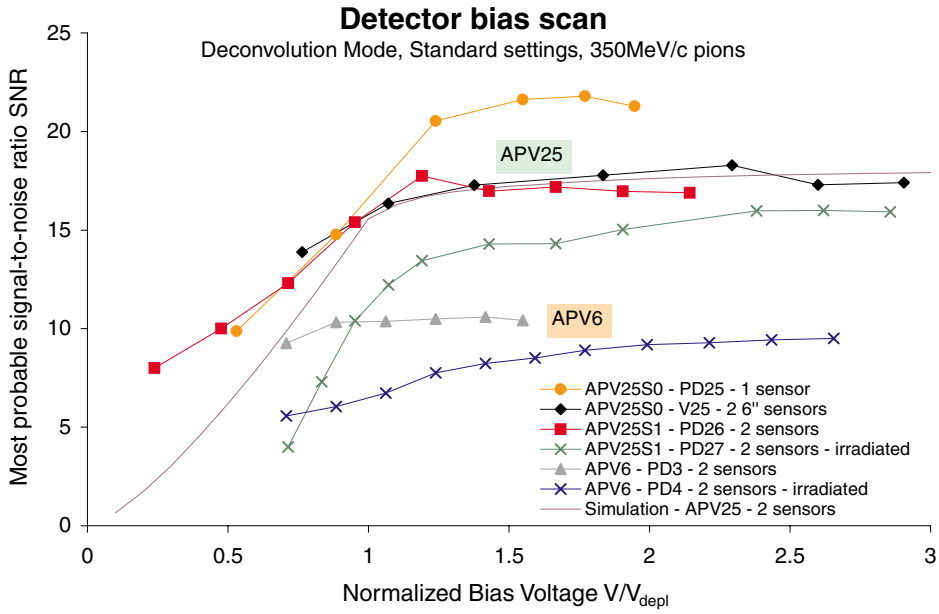



Figure 5.22: Deconvolution signal-to-noise ratio of different silicon detector modules as a function of the detector bias normalized to the respective non-irradiated depletion voltage.

Moreover, the SNR was measured as a function of the particle hit position on the detector along the strip axis. Again, no difference could be observed between hits close to and far from the amplifier chips. Since the particle induced signal is current driven, it does not depend on the series line resistance between hit position and amplifier input, while the noise performance is independent of particles anyway. Thus, the signal-to-noise ratio is not affected by the hit position on the detector.

An angle scan was performed with the Vienna APV25 module outside of the cooling box. The results obtained here are compatible with previous measurements discussed in section 5.1.3, p. 81, and the same fit functions have been applied. Fig. 5.23 shows signal (top) and cluster width (bottom) as functions of the incident angle for both pions and protons, where an angle of zero denotes perpendicular incident.

While the signals of the detector modules were usually read out by a copper cable with a length of 25 m, a prototype of the analog optical link (see section 5.2.1, p. 113), with 97 m of optical fiber was used instead of the cable for comparative measurements. In general, the same signal-to-noise ratio was measured with cable and optical fiber. This is because the long cable brought a bandwidth limitation which led to a slight signal reduction compared to a short cable. The optical link has a significantly higher bandwidth but contributes additional noise. These effects approximately compensate each other, yielding similar results in both cases.

For a short period, the setup was modified in such a way that the APVs were directly clocked with the 50 MHz PSI frequency and thus, the synchronization module could be abandoned. In peak mode, the performance remained unchanged, while in deconvolution mode a signal loss of approximately 13% was observed due to the static weights of the signal processing algorithm which are laid out for 40 MHz operation (see section 2.6.3, p. 35). This loss has been confirmed by simulation.

#### 5.1.5.3 High Intensity

As pointed out earlier, the scintillator trigger functionality is reduced at high intensity, as particles arrive with every bunch. The difference between scintillator and random triggering at a beam intensity of 1.4 MHz is illustrated in fig. 5.24. It shows the number of measured hits per strip in the Vienna Milestone module. The last two APV6 chips were not fully functional, so their strips are not included in this plot. Regardless of the trigger type, the wide-spread high intensity beam causes a pedestal of approximately 80 hits in every channel. With the beam trigger, the hits in the area covered by the scintillator are preferredly read out, but other particles contained in the same bunches still produce the same background. At low intensity, the beam profile is the same but reduced by the background level.

The absolute particle flux is proportional to the measured hit profile with random trigger. However, it is difficult to state the proportionality factor. First of all, our high intensity measurements had an enormous dead time. Further triggers were blocked until the computer finished reading out the previous event data from the ADCs, which took about 5 ms. With particle bunches arriving every 20 ns, the sensitive time window is only 4 ppm. An uncertainty of the actual readout time propagates to this fraction. Moreover, the hit discrimination strongly differs between peak and deconvolution modes resulting in different time over threshold windows, which also depend on the signal amplitude and the timing with respect to the APV clock. Thus, we relied on the scintillator for the beam intensity measurements.

The statistical character of the high intensity PSI pion beam was also verified by the distribution of the number of hits per time slot. For better statistics, this measurement has been

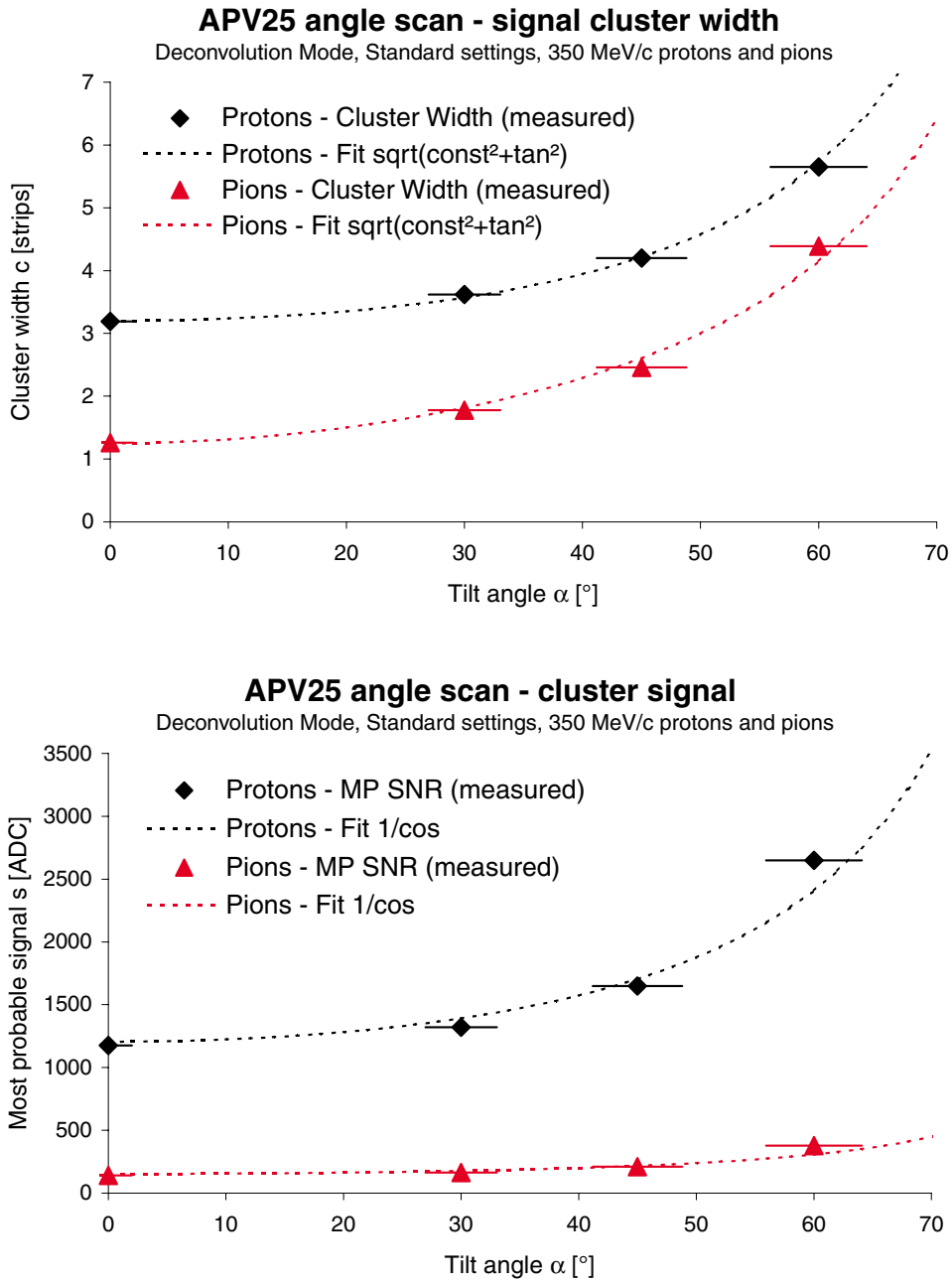



Figure 5.23: Angle scan of the Vienna APV25 module. Both cluster signal (top) and cluster width (bottom) increase with the incident angle.

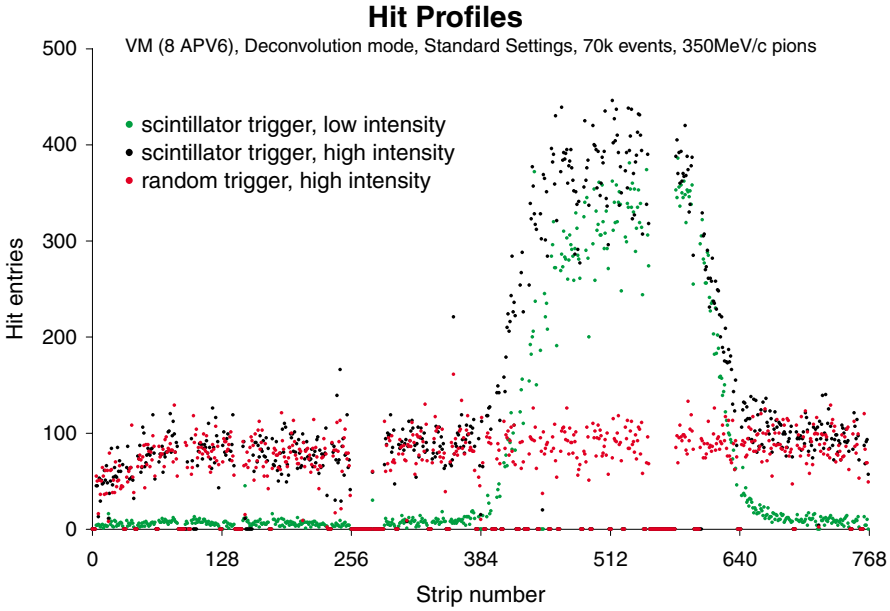



Figure 5.24: Measured hit profiles at low intensity with scintillator trigger (blue) and at high intensity with scintillator (black) and random (red) triggers.

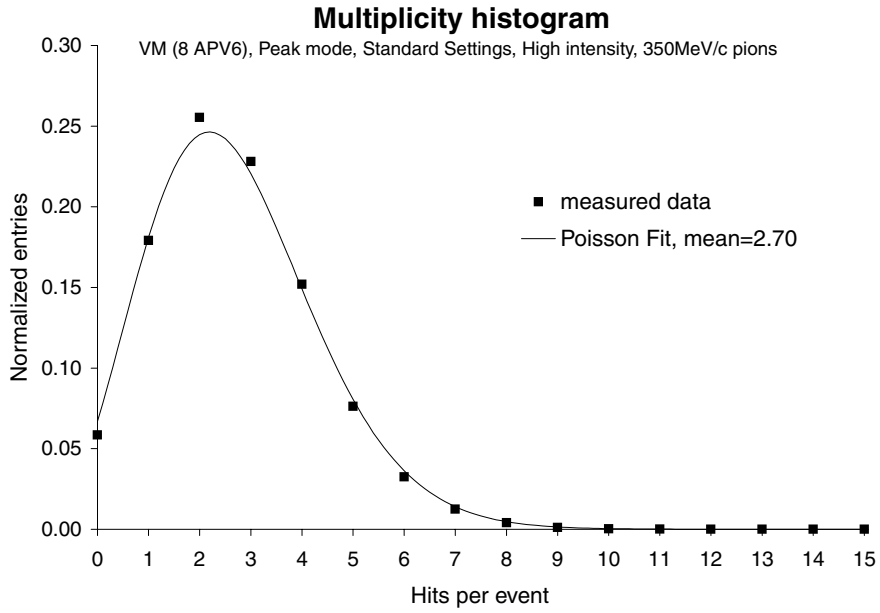



Figure 5.25: Measured distribution of the number of hits per random trigger at high intensity in peak mode, fitted by a Poisson distribution.

performed in peak mode, where the time window is open longer for particle hits than in deconvolution mode. Fig. 5.25 shows the multiplicity distribution obtained from the Vienna Milestone module at high beam intensity. The good agreement with the Poisson distribution demonstrates the highly random nature of the beam.

Apart from the above investigations, normal runs have been made during a period of more than 24 hours at high intensity. The module performance remained unchanged during these runs compared to low beam intensity.

Since the detector currents were continuously monitored, the leakage current increase could be observed as a function of total dose. This is best demonstrated by the Vienna APV25 module, which had an extremely low initial leakage current. Fig. 5.26 shows the current development of the V25 module at $-10°$ C at high beam intensity.

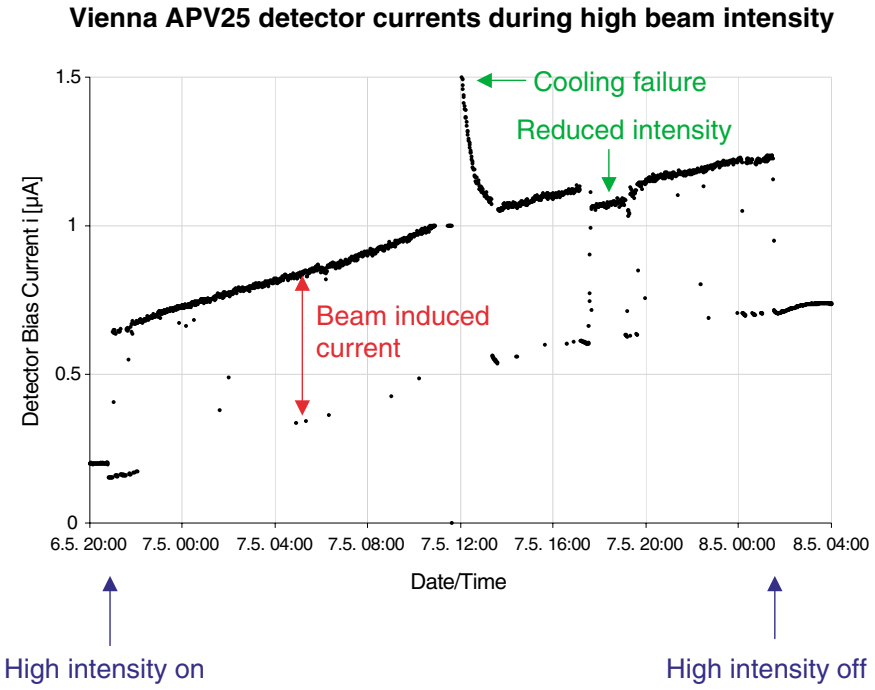



Figure 5.26: Detector current of the V25 module during the high intensity period.

Initially, the current is very low, but jumps by approximately 0.5 $\mu$A as soon as the high intensity beam is turned on. This is caused by the large number of carriers generated within the detector by the crossing particles, therefore called "beam induced current". Although the current contribution of a single particle is very small and of short duration, as demonstrated by the detector simulation discussed in section 2.2, p. 17, the huge number of particles over the large area of the two sensors result in a significant DC current which has to be delivered by the power supply.

The slope of the current in fig. 5.26 corresponds to the increase of leakage current caused by radiation defects (see section 2.3.2, p. 26). A current related damage rate of $\alpha \approx 8 \cdot 10^{-17}$ A/cm at room temperature has been extracted from this measurement, which agrees with values given by the RD48 collaboration [22].

Occasionally, the beam went off for a few seconds, resulting in a measurement of the pure leakage current without the beam induced component. Joining these points would result in a

parallel line of the same slope but at lower level. The current peak in the center was resulting from a power failure of the slow control computer, thus switching off the cooling for half an hour. During this period, the temperature in the cooling box warmed up to 0° C, resulting in a dark current increase by a factor of 2.7 according to eq. 2.27, p. 26, which was actually observed. After restoring the operating temperature, the current curve continues unaffected. Later, the beam intensity was slightly reduced for about two hours, resulting in a lower beam induced current.

#### 5.1.5.4 Multi-Peak Mode

As pointed out in section 5.1.1.2, p. 74, the APV Sequencer is able to generate a programmable trigger pattern which is issued either by software or hardware trigger. Together with the multi-peak mode of the APV25, this feature can be used to effectively obtain subsequent samples of the shaping curve from a particle signal.

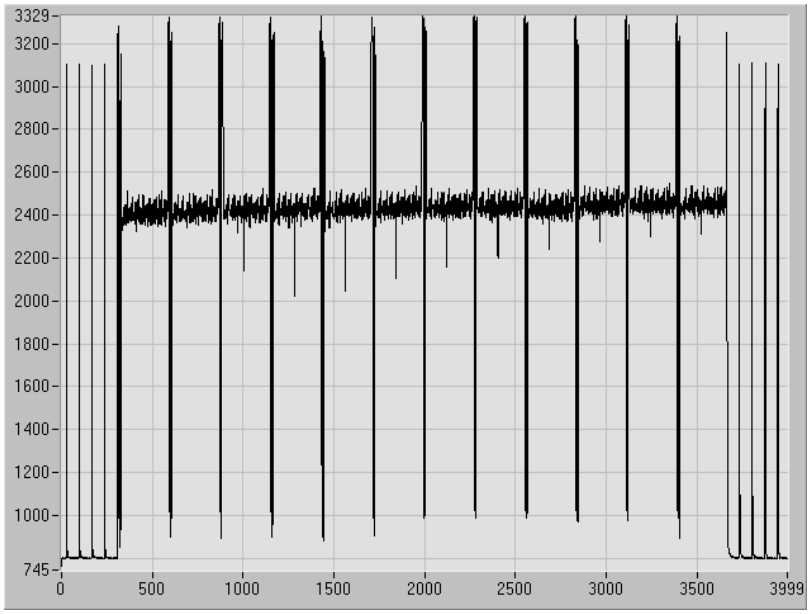



Figure 5.27: Screenshot of the raw APV25 output with consecutive samples obtained with a trigger sequence in multi-peak mode, representing a single particle hit.

Fig. 5.27 shows an example of the APV25 output in this mode. Four triggers separated by 75 ns are sent to the APV25, which returns three consecutive samples after each trigger, resulting in a total of twelve sequential samples, revealing the (negative) pulse shape. The average waveform obtained from this measurement matches with the peak mode pulse shape scanned by internal calibration.

A pulse shape fit has been applied to every multi-event, returning the peaking time position. With the normal scintillator trigger, the distribution of these peaking times are an indicator for the quality of timing and synchronization. As shown in fig. 5.28, an RMS peaking time spread of 2 ns was obtained, including beam fluctuations, the timing jitter and the fit error.

The same measurement was repeated at high intensity with random triggering. With the APV25 still clocked at the nominal 40 MHz, the PSI beam structure of 50 MHz (corresponding to 20 ns) is visualized (fig. 5.29). The pulse shape fit does not always converge. With a later peak,

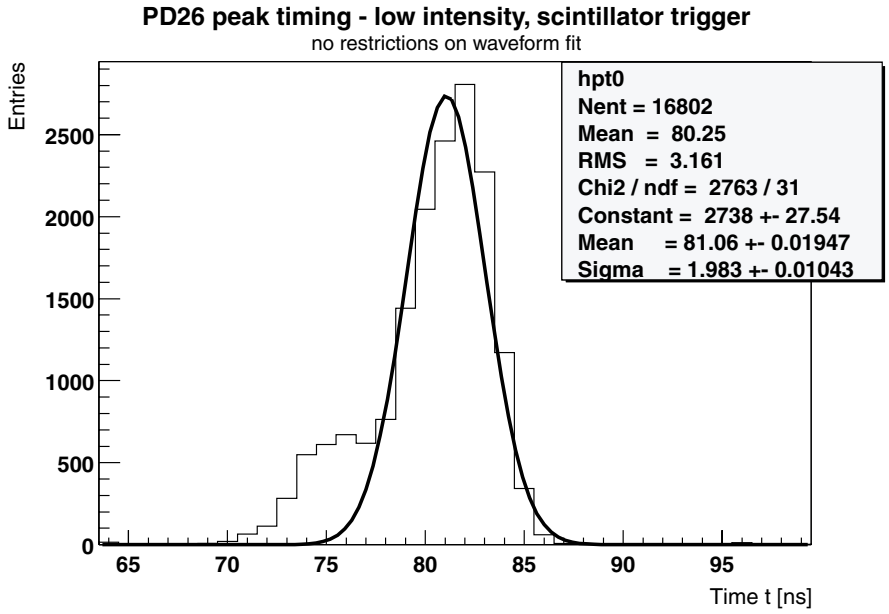



Figure 5.28: APV25 peaking time distribution with scintillator trigger at low intensity.

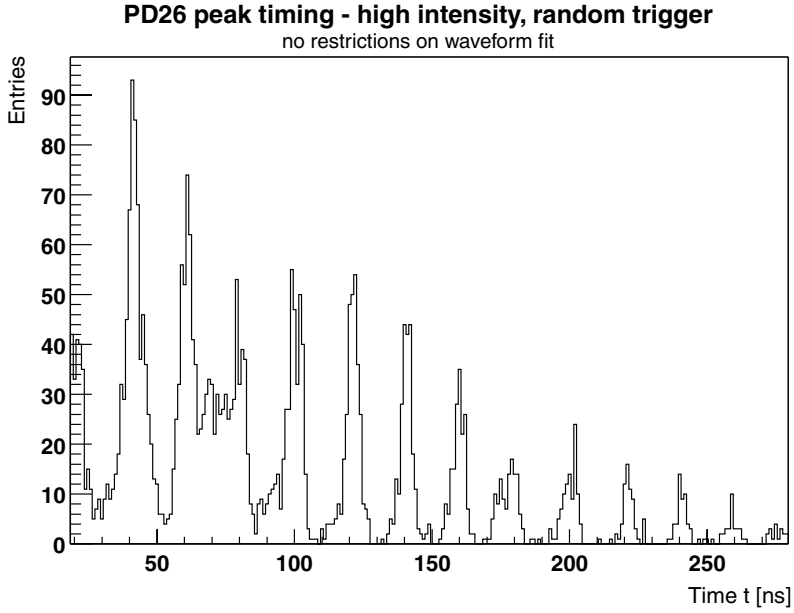



Figure 5.29: APV25 peaking time distribution with random trigger at high intensity, revealing the 20 ns PSI beam period.

less signal samples are contained within the measurement window, making the fit procedure more difficult. Fits which did not converge were not included in this plot, leading to fewer entries with increasing peaking times, although the peaking times are evenly distributed over the full scale.

### 5.1.6 APV25 Irradiation (December 2000)

In December 2000, APV25S1 chips were placed in an intense particle beam at PSI [65] to study the effects of radiation. A total dose of $1.87 \cdot 10^{14}\,\pi^+\,\mathrm{cm}^{-2}$ was achieved with positive pions at a momentum of 300 MeV/c. This dose slightly exceeds the total expected hadron fluence in the innermost layer of the CMS Silicon Strip Tracker over 10 years. The flux achieved in the PSI test was approximately $10^9\,\pi^+\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$ and thus about 1000 times higher than during CMS operation. The nuclear interaction cross-section of positive pions on protons peaks at 300 MeV/c, which makes them ideal for such a test.

Of the radiation effects described in section 2.6.5, p. 38, a large number of single event upsets (SEUs) was measured, but also an effect which might come from oxide charging. No single event latchup or gate ruptures were observed. The digital SEU rates will be compared to the results of a similar test with heavy ions, concluded with a prediction for the rates in the CMS tracker.

Additional information on the SEU test can be obtained at [12].

#### 5.1.6.1 Setup

A stack of eight APV25S1 chips (fig. 5.30) were placed in the beam focus. The hybrid for the chips was especially designed for this test, containing no passive elements except decoupling capacitors. This was done because the intention was to test the APVs and not other devices under irradiation, while the capacitors were known to be radiation tolerant. The chips had no detector connected and the stack was placed in the cooling box at an ambient temperature of $-10°$ C.

The APV chips were read out by the same hardware as used in module tests. For the front-end, a special backplane board was developed to connect the eight hybrids. Clock and trigger lines, which are normally terminated on the hybrid, were returned to the backplane and terminated there. An external calibration line was included but finally not used because of excess noise. An additional feature of the backplane was the possibility to monitor all supply voltages and currents.

Some of the chips should have had their output being transmitted over a new, radiation tolerant prototype of the analog optical link placed in the beam as well, but unfortunately this prototype was not fully functional, such that the data were entirely transmitted over cable.

Moreover, the PSI cyclotron system had massive problems at that time, such that only a fifth of the targeted fluence of $10^{15}\,\pi^+\,\mathrm{cm}^{-2}$ could be achieved – nevertheless, good statistics and consistent data were obtained from this test.

Apart from the APV25S1 chips, commercial digital optical transceivers, three silicon detector modules and submicron test structures were irradiated in this beam, but their results will not be discussed here.

#### 5.1.6.2 Measurement Procedure

The measurement procedure for the SEU test differs from the module tests. Fig. 5.31 shows the software flow for the single event upset measurements. In the beginning, both hard and soft

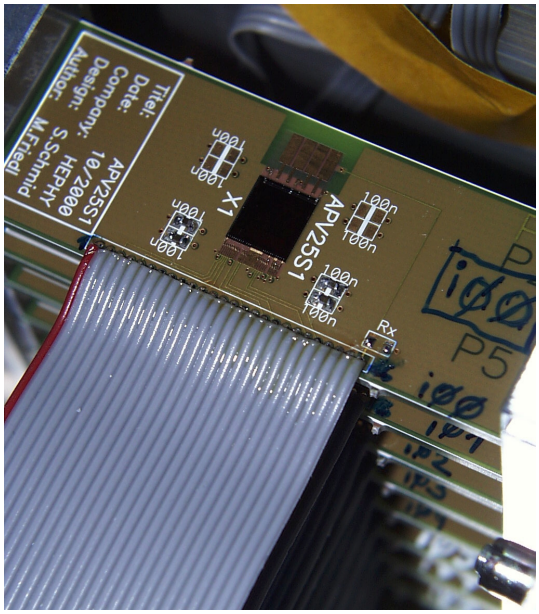



Figure 5.30: Stack of eight APV25S1 chips in submicron technology prepared for the irradiated in a pion beam.

resets are applied to the APV chips, the registers are loaded over the $I^2C$ bus and pedestals and noise are evaluated as it is done in the module tests. Then, different tests are performed in a loop until an error is detected. These measurements include several thousand software-triggered events with and without internal calibration. The APV voltages and currents are measured at one point in the cycle, and the APV register settings are read back over the $I^2C$ bus. Moreover, the digital optical transceivers (DOT) are tested.

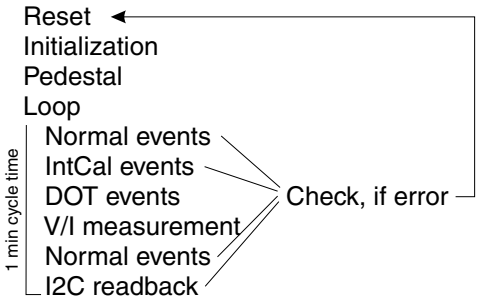



Figure 5.31: The principal measurement procedure for the SEU test.

Thus, data are continuously read out with a cycle time of approximately one minute. Each single APV event is subjected to a few checks:

- Is the data frame complete?
- Is the error bit set?
- Is the pipeline address synchronous with the other APVs?
- Do the analog data make sense?

In very rare cases, the entire frame may be missing after a digital SEU in the control logic. When this is not the case, the error bit has to be checked. If it is set, the APV error register can be read over $I^2C$ to distinguish between latency and FIFO errors. The error bit indicates about 81% of all digital single event upsets. Another 15% are detected by matching the pipeline addresses between the APVs on a single hybrid. Since those are run from the same clock and trigger lines, they ought to run synchronously unless a SEU causes an error in the pipeline logic. Approximately 4% of the digital single event upsets flip a bit in the $I^2C$ registers. This condition cannot be safely detected in the output data frame. Either is does virtually no harm (e.g., when the LSB of a register flips), or it affects the signal amplification but not the pedestal output (e.g., by changing of bias voltages or currents in the preamplifier section), or it obviously affects the output (e.g., by shifting the pedestals). A quality check of the analog data should be able to detect at least some of those SEUs. To be sure, one has to read back the $I^2C$ registers and compare them to the set values.

These simple software checks (without $I^2C$ readback) should be implemented whenever the risk of data corruption by SEUs exists. In particular, this appears to be necessary in the CMS data acquisition to discard wrong data.

In addition, the analog data are checked for unexpected hits, which indicate analog SEUs. In case of an error, it is analyzed, counted and logged, and the loop execution is stopped. The program starts over with sending resets and reinitializing the APVs.

The major part of the SEU tests was performed in deconvolution mode with a medium pipeline latency (98) at $-10^\circ$ C. However, data were also obtained in peak mode, at high latency (187) and at room temperature.

#### 5.1.6.3 Digital SEUs

The SEU cross-section $\sigma$ is defined by the number of upsets $N$ divided by the fluence $\Phi$ accumulated during the measurement time,

$$\sigma = \frac{N}{\Phi} \quad . \tag{5.3}$$

If an electronic structure was fully sensitive to every crossing particle, the cross-section would equal the physical area of the structure. In reality, this certainly never is the case. In particular, the ionization potential of pions is by far too low to generate a single event upset. Only secondaries, such as recoil atoms produced within the sensitive layer, can achieve this condition.

More than 3000 single event upsets were observed in total during this pion irradiation with a cross-section slightly depending on the temperature. Tab. 5.5 compares the results for warm and cold operation. The SEU cross-section at the operating temperature of $-10^\circ$ C will be used for further calculations. No dependence of the digital SEU rate on mode or latency settings was measured.

| **Temperature** [° C] | **SEU cross-section** [$cm^2$] |
|---|---|
| +20 | $1.99 \cdot 10^{-12}$ |
| -10 | $2.25 \cdot 10^{-12}$ |

Table 5.5: Digital SEU cross-section of 300 MeV/c $\pi^+$ on the APV25S1.

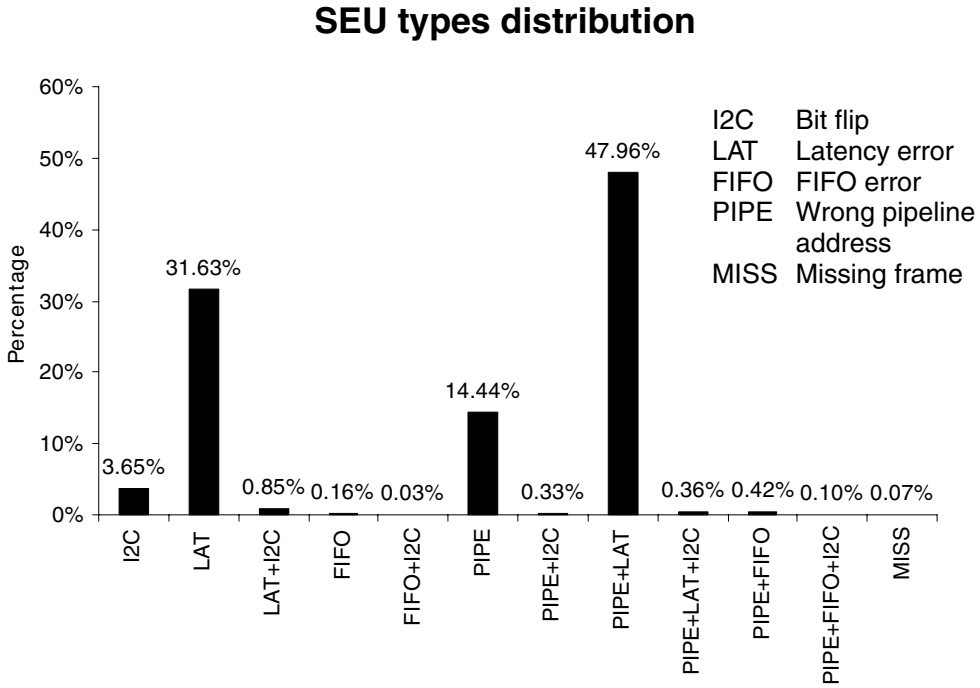



Figure 5.32: Distribution of digital single event upsets.

Each SEU can result in one single effect or a combination of effects detected by the software checks. Fig. 5.32 shows the distribution of all observed combinations of digital single event upsets.

Each SEU can be assigned to one of three digital blocks, which are pipeline and control logic, the FIFO logic or the $I^2C$ registers. The SEU cross-section of each block is compared to the actual sensitive area on the chip in fig. 5.33, revealing principal agreement. More than 96% of all SEUs are pipeline related, corresponding to the largest digital block in the physical layout of the chip.

The statistical nature of SEUs can be shown by their waiting time distribution (fig. 5.34). Ideally, this distribution should follow an exponential decay. However, the measurement procedure did not allow continuous SEU detection. During the digital optical transceiver tests and the measurement of voltages and currents, which took about 15 s together, the APVs were not read out and thus no SEUs could be detected during that period. The hole between 30 and 45 s in fig. 5.34 corresponds to this dead time. SEUs produced within this period were detected immediately after finishing the other measurements, leading to the peak after the hole. The hole and peak structure repeats with a period of one minute due to the cycling measurement procedure. Apart from this artefact, the waiting time distribution demonstrates the random appearance of single event upsets.

When a single event upset occurs, the next data frame is corrupted. If the error bit is set, the same frame data are returned with future triggers until the chip receives either hard or soft reset. Bias registers which have been corrupted by a SEU may or may not affect the data. Thus, it seems advantageous to send a reset and reload the registers from time to time. All SEUs observed in this test could be cleared by a combination of hard and soft reset; no permanent effects were detected.

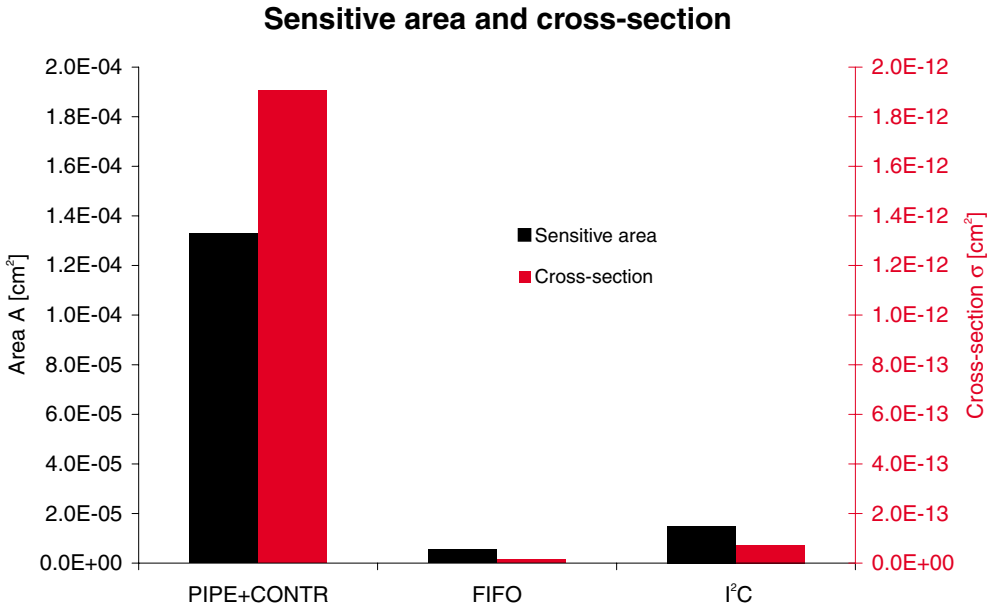



Figure 5.33: Digital SEU cross-section and sensitive area for three different logic blocks on the APV25S1.

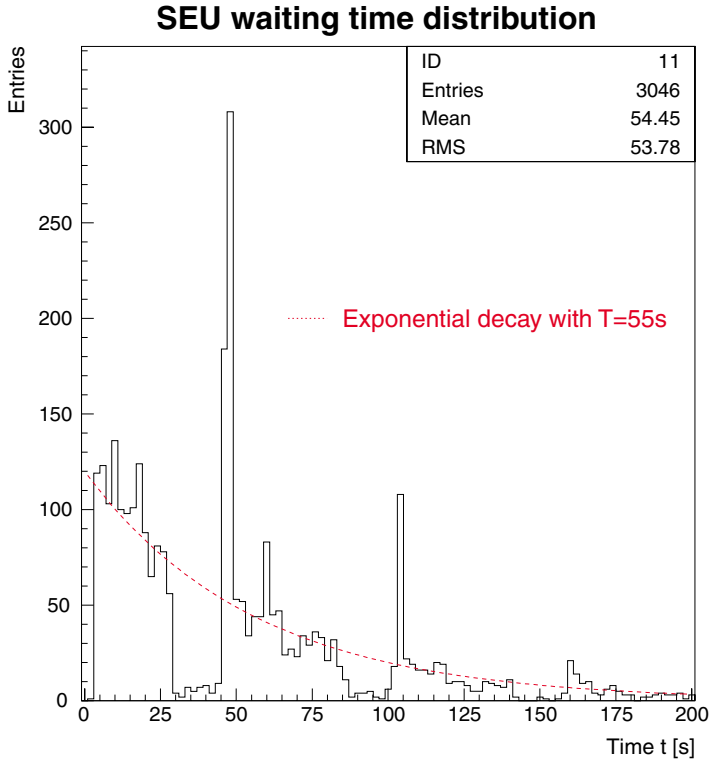



Figure 5.34: Waiting time distribution between two digital SEUs in any of the eight APV25S1.

A similar test has been performed with heavy ions [66]. By variation of the ions and their energy, the threshold energies required to generate various types of single event upsets were measured. Fig. 5.35 compares the cross-sections obtained by heavy ions to the pion results. The $I^2C$ register cross-section has been split into bit errors in either direction. The factor of approximately $10^8$ between heavy ions and pions reflects the fact that only secondary particles generated by a small fraction of pions cause a single event upset.

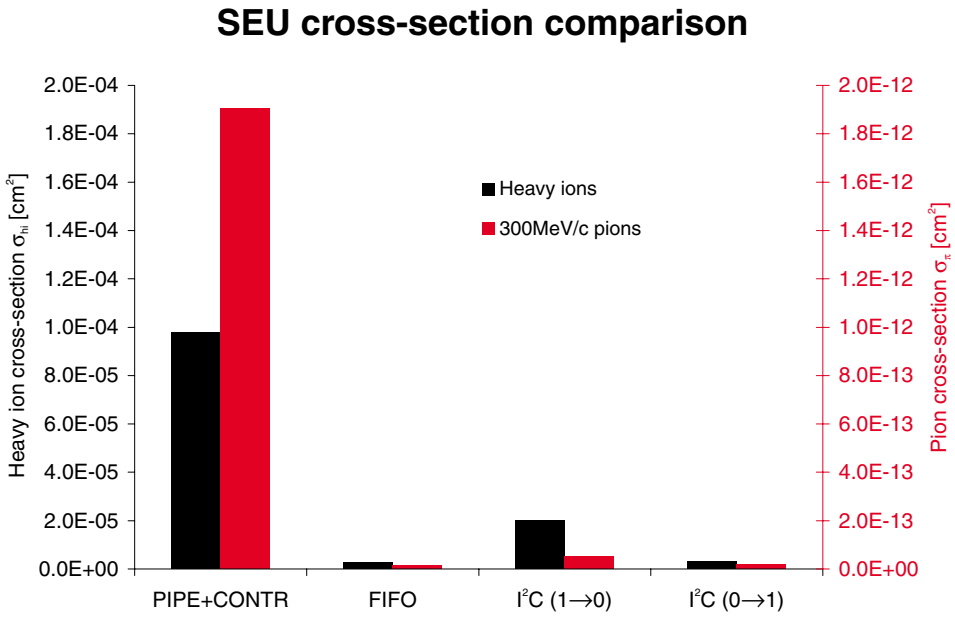



Figure 5.35: APV25 digital SEU cross-section comparison between heavy ions and pions.

#### 5.1.6.4 Analog SEUs

Similar to the flipping of a digital cell, a heavily ionizing fragment can deposit charge on a pipeline capacitor, thus producing a fake hit. The probability of such an analog single event upset is much higher than that of the digital counterpart, since the sensitive area of the pipeline is larger and there is no threshold for the charge deposition.

For practical detection of analog SEUs, a threshold must be defined in order to distinguish true single event upsets from noise. A safe threshold of $40\,\sigma$ (i.e., forty times above the RMS noise level of each channel) has been selected in the SEU tests. This threshold corresponds to charges of approximately 16000 e and 11000 e in deconvolution and peak modes, respectively.

Analog single event upsets of either polarity have been observed, slightly dominated by positive signals. Fig. 5.36 shows a typical pulse height spectrum.

The mean amplitude of the positive signals and the measured cross-sections with three different settings are plotted in fig. 5.37.

The analog SEU cross-section with a $40\,\sigma$ cut is a few times higher than its digital counterpart, but is expected to be much higher with a lower threshold. It rises with increasing latency, since the sampled shaper output longer remains in the pipeline and thus each cell is exposed to potential charge deposition for a longer time span.

The measured cross-section in peak mode is higher, because the $40\,\sigma$ threshold corresponds to a lower charge, resulting in a larger number of recognized fake hits. At the same time, the average

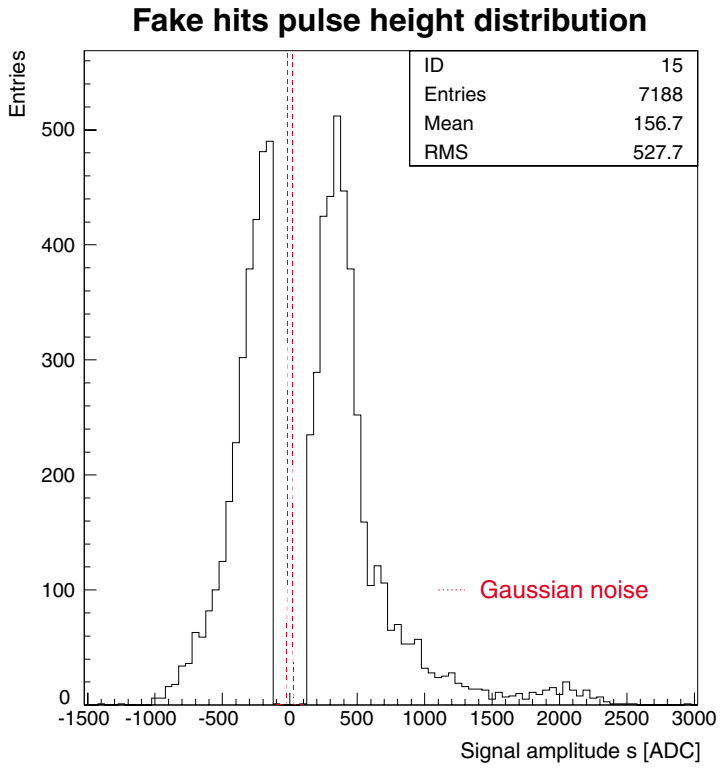



Figure 5.36: Typical pulse height distribution of analog SEU signals. The central peak shown in red represents the Gaussian noise distribution, which is entirely excluded by the $40\,\sigma$ cut. The calibration for the signal amplitude is approximately 75 e/ADC.

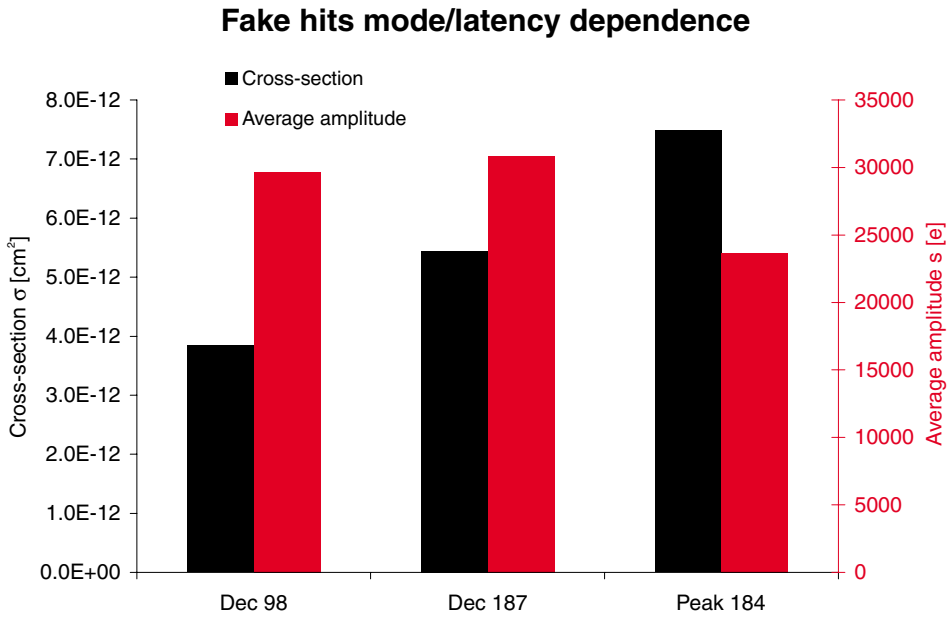



Figure 5.37: Mean amplitudes of positive fake hits and total cross-sections measured on the APV25S1.

charge figure decreases due to the lower threshold. Considering these measurement artefacts, both the cross-sections and the amplitudes are compatible between peak and deconvolution modes at similar latency.

Although the probability of an analog single event upset is much higher than the digital SEU cross-section, it does not need any action to be cleared. Since the pipeline is constantly refreshed with a period of the latency, affected cells are automatically overwritten by other samples. Despite the higher cross-section, the number of fake hits is still negligible compared to the overall amount of data.

#### 5.1.6.5 Other Results

No irregularities were observed on the supply voltages and currents. In fact, this would only be the case with a single event latchup or gate rupture, when a conductive path between supply rails was created.

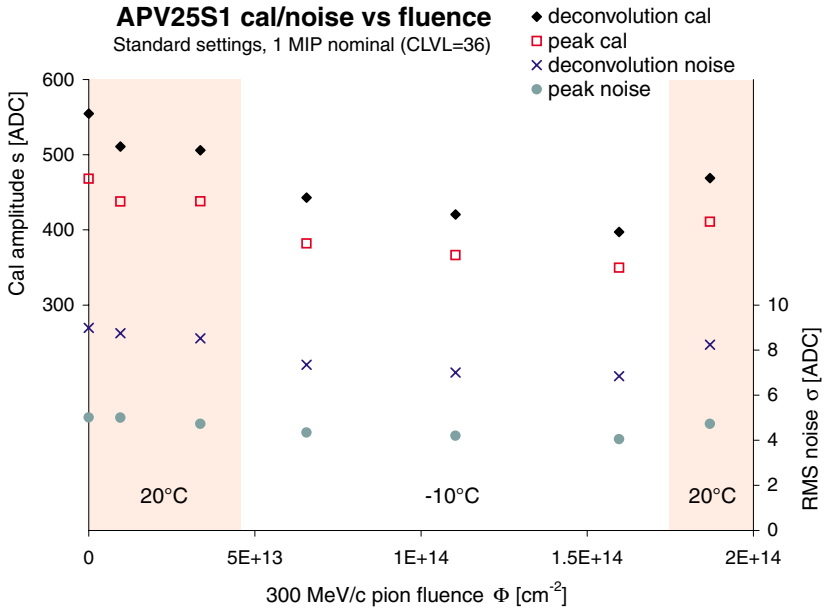



Figure 5.38: Amplitude of the internal calibration pulse vs. the total fluence. The data within the shaded areas were measured at room temperature, while the central part was obtained at $-10°$ C.

Internal calibration measurements were performed periodically when the beam was off. Fig. 5.38 shows the amplitude of the internal calibration signals in both peak and deconvolution mode and the noise over the accumulated fluence. The APV chips revealed a small temperature dependence, which is common for semiconductors. Apart from that, a minor decrease in the amplitude of about $-15\%$ relative to the initial value was obtained at the final fluence of $1.87 \cdot 10^{14}\,\pi^{+}\,\mathrm{cm}^{-2}$.

The noise values however show the same development for both fluence and temperature, such that the signal-to-noise remains unaffected. Thus, this effect purely is a matter of gain. Oxide charging is the suspected reason of the gain degradation, but this is not yet confirmed and needs further investigation.

#### 5.1.6.6 CMS Prediction

A prediction of single event upsets for the CMS tracker includes several assumptions and thus implies a large error bar. First of all, the flux or integrated fluence as a function of radius and rapidity is not exactly known. Moreover, the particles expected in CMS are not mono-energetic, and of various types. Simulations [7] predict that the particle zoo is dominated by charged hadrons, especially pions, with a momentum below 1 GeV/c. Regarding the nuclear interaction cross-section resonance peak of 300 MeV/c pions on protons [3], a straight SEU extrapolation is likely to result in an overestimation.

The heavy ion results suggest a cross-section of approximately $10^{-12}\,\mathrm{cm}^2$ for the CMS environment, which is in fact half the value measured with pions. Thus, the direct extrapolation of the pion results can be considered as a worst case scenario.

The average flux in the CMS tracker has been derived from a simulated radiation profile and an integrated luminosity of $5 \cdot 10^5\,\mathrm{pb}^{-1}$ over $5 \cdot 10^7$ s. The analog SEU rate has been interpolated for a latency of 127 in deconvolution mode with a first level trigger rate of 100 kHz. A total cross-section of $4.36 \cdot 10^{-10}\,\mathrm{cm}^2$, which is 100 times higher than the cross-section measured with a $40\,\sigma$ threshold, has been assumed to include fake signals of low amplitude. Tab. 5.6 shows the average SEU rates for inner and outer barrel sections of the CMS tracker. As mentioned above, these numbers are derived from the pion cross-sections and should rather be considered as an upper limit. Due to large uncertainties, they merely indicate the order of magnitude of SEU rates which one can expect at CMS.

| **Section** | **Avg. flux** [$\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$] | **Number of APVs** | **Mean dig. SEU time** [s] | **Dig. SEUs/ time** [$\mathrm{h}^{-1}$] | **Mean analog SEU time** [s] | **Analog Occupancy** |
|---|---|---|---|---|---|---|
| IB | $1.40 \cdot 10^6$ | 14400 | 22.1 | 162.7 | 0.11 | $6.88 \cdot 10^{-7}$ |
| OB | $4.85 \cdot 10^5$ | 29232 | 31.4 | 114.7 | 0.16 | $4.84 \cdot 10^{-7}$ |

Table 5.6: Extrapolation of the pion SEU cross-sections to CMS. Due to large uncertainties, these numbers only indicate the order of magnitude. The analog occupancy gives the probability of an analog SEU on a single channel.

Neither the digital nor the analog SEU rates pose a threat to CMS. A general reset with subsequent reprogramming of the APV chips should be performed periodically, and the DAQ software should mask wrong data from upset chips until the next reset. The number of analog SEUs is completely negligible, since less than one data sample in a million contains a fake hit. This can be regarded as a marginal increase in the noise background.

### 5.1.7 APVMUX Test (February 2001)

A hybrid containing six APV25S1 chips and the APVMUX was designed and assembled at Strasbourg. Apart from minor details, this is the final hybrid for the CMS tracker, shown in fig. 5.39 with an attached kapton cable. The analog output of the six chips is multiplexed onto three lines by the APVMUX, which is the narrow chip in the center of the hybrid.

The behavior of the hybrid and in particular the APVMUX was evaluated at HEPHY [67]. Since the multiplexed APV25 output is clocked at 40 MHz, the input stage of the VME-ADC was modified by removing a slow amplifier, thus increasing the $-3$ dB bandwidth from 50 to 90 MHz.

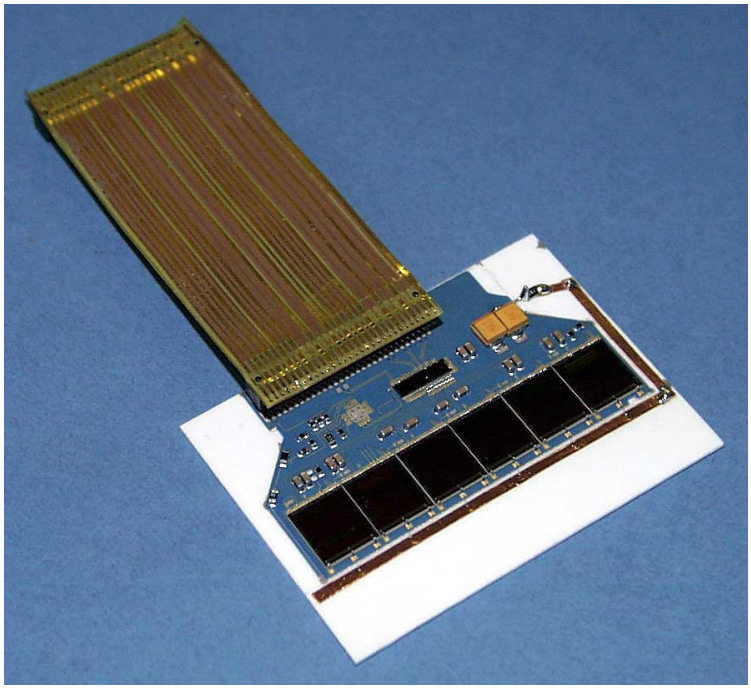


Figure 5.39: The close-to-final hybrid with six APV25S1 and an APVMUX.

#### 5.1.7.1 Calibration and Noise

Signal and noise resulting from internal calibration measurements with a nominal amplitude of 1 MIP (22500 e) are shown for both peak and deconvolution modes in tab. 5.7. No capacitive load was connected to the APV inputs. The noise figures obtained here still include a small contribution of the readout system. On the other hand, the internal calibration is known to produce signals which are larger than their nominal values (see section 5.1.4.1, p. 85), thus resulting in a noise underestimation. Assuming that these effects approximately compensate each other, the numbers given here are compatible with the values obtained for a single APV25S1 (tab. 5.2, p. 86). Thus, the APVMUX does not contribute significant noise.

| **Mode** | **Signal** [ADC] | **Noise** [ADC] | **SNR** | **Noise** [e] |
|---|---|---|---|---|
| Peak | 72 | 1.10 | 65.5 | 344 |
| Deconvolution | 83 | 1.58 | 52.5 | 428 |

Table 5.7: Internal calibration signal and noise measurements on an APV25S1 followed by the APVMUX.

#### 5.1.7.2 Crosstalk

The crucial characteristic of the APVMUX is its switching speed. If the switches were too slow, a signal in one chip would drop its shadow in the second chip data. To test the APVMUX switching behavior, the even APV25 was pulsed with internal calibration, while the odd chip, connected to the same multiplexer channel, remained at pedestal level (see section 4.2.1, p. 63, for APVMUX details). Fig. 5.40 shows the corresponding output of the APVMUX after amplification by

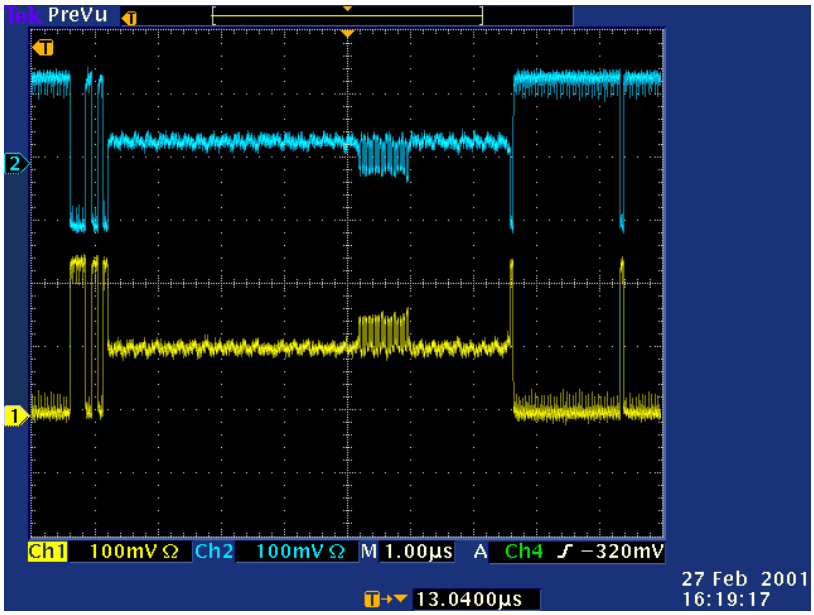



Figure 5.40: Positive (bottom) and negative (top) outputs of the APVMUX after amplification by the repeater. A group of channels on the even APV is internally pulsed.

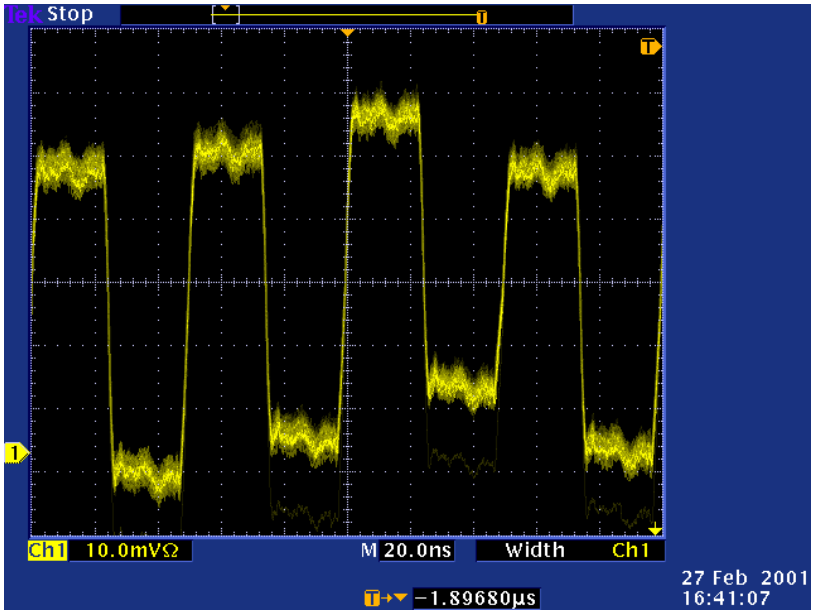



Figure 5.41: Zoomed view of the APVMUX switching between pulsed and non-pulsed APV channels.

the repeater board. This oscilloscope screenshot is the measured equivalent of fig. 4.17, p. 63. Zooming into the region of the pulsed channels, it is obvious that the switching procedure is extremely fast and precise (fig. 5.41). A rise time of approximately 3 ns has been measured, including the amplifier on the repeater board and the oscilloscope, which actually account for the major fraction of this value.

The crosstalk of signals on the even chip onto the odd has also been measured and quantified with the APV readout system. As expected from the oscilloscope screenshots, virtually no crosstalk was observed with this measurement. Fig. 5.42 shows the internal calibration waveforms in deconvolution mode for both pulsed (black) and adjacent (red) channels.

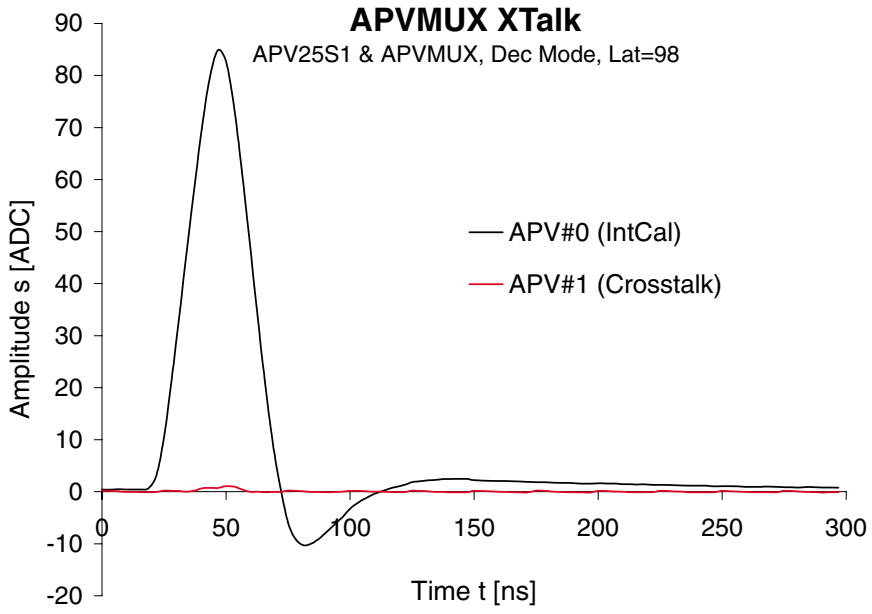



Figure 5.42: Averaged internal calibration waveform of the even APV25S1 chip (black) and the negligible crosstalk in the neighboring channels of the odd chip (red).

The relative crosstalk amplitudes (tab. 5.8) are about 1% and thus negligible, since the noise level is about one order of magnitude higher. For comparison, a crosstalk in the order of 5% was obtained with the 50 MHz bandwidth ADC version because of slower transients.

| Mode | Relative crosstalk |
|---|---|
| Peak | 0.7% |
| Deconvolution | 1.2% |

Table 5.8: Relative crosstalk amplitudes observed in the odd APV when pulsing the even chip.

### 5.1.8 APV25 Magnetic Field Test (March 2001)

The behavior of APV25S1 and optical lasers (see section 5.2.2, p. 116) was tested in a strong magnetic field in collaboration with the Institute of Material Physics at the Vienna University [68]. The helium-cooled, superconducting magnet provides a homogeneous flux density of up to 14 T. Our tests were performed in the regime of 0 up to 10 T, where handling is much

easier at reduced helium consumption. Moreover, the magnetic field in the CMS tracker is only 4 T.

An APV25S1 chip was positioned in three orthogonal orientations with respect to the magnetic field. These positions are denoted A, B and C in fig. 5.43. The mechanical support is designed to fit into the magnet core which is 3 cm in diameter.

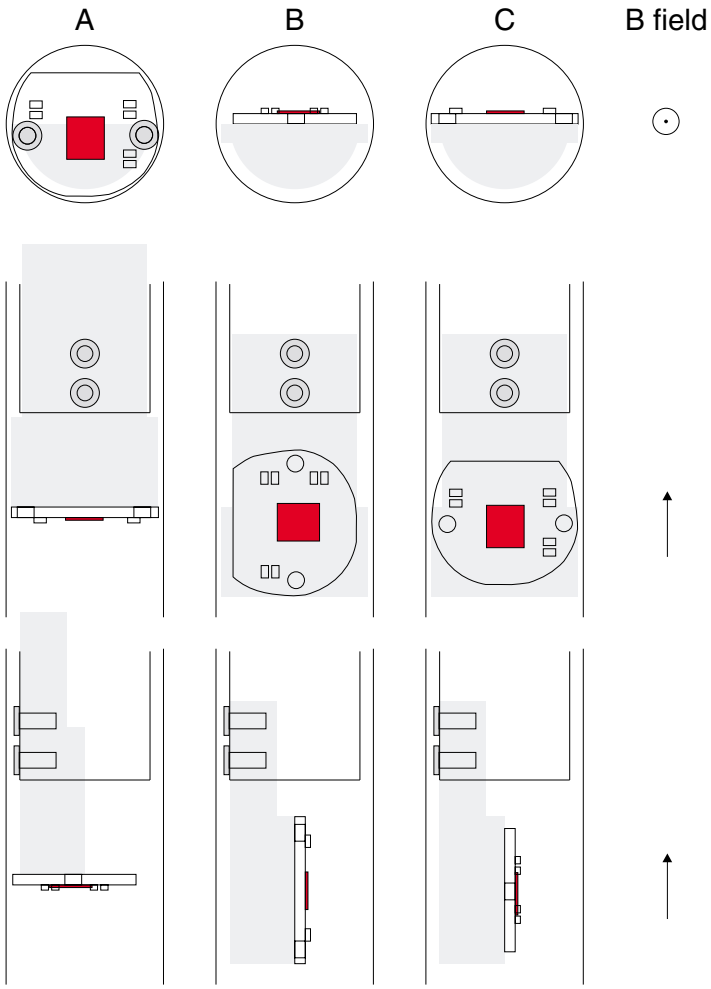



Figure 5.43: The three different orientations (A, B and C) of the APV chip (red) with respect to the magnetic field.

Noise, internal and external calibration were measured at 0, 4 and 10 T. The presence of the magnetic field was easily observed on the cathode ray tube (CRT) monitor, which was located in the stray field about 2 m away from the magnet. The distorted image of the DAQ software is shown in fig. 5.44.

The APV performance was completely indifferent to the presence of a magnetic field. Fig. 5.45 shows an overlay plot of the internal calibration waveform in deconvolution mode for the three different orientations (A, B and C) and magnetic fields between 0 and 10 T. The average noise deviation between any two measurements was less than 2%, which is the usual tolerance and not related to the magnetic field.


Figure 5.44: Image of a CRT monitor, located approximately 2 m away from the magnet coil with an inner flux density of 10 T. The magnetic field not only rotates the picture geometry, but also disturbs the color representation.

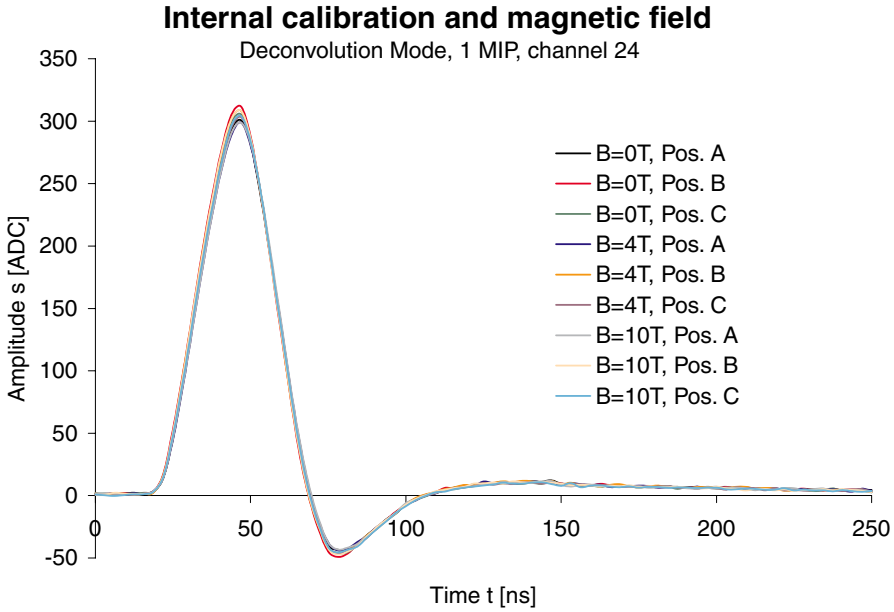



Figure 5.45: Overlay plot of the internal calibration waveform in deconvolution mode for the three different orientations (A, B and C) and magnetic fields of 0, 4 and 10 T. Obviously the APV chip is not affected by a magnetic field.

## 5.2 Analog Optical Link Tests

### 5.2.1 Analog Optical Link Laboratory Tests (September 1999)

In autumn 1999, we received a prototype of the analog optical link with four channels. It consists of a laser driver optohybrid, which converts electrical to optical signals with a bias programmable over its $I^2C$ interface. On the other end of approximately 100 m of a 4-way optical fiber, a receiver hybrid provides an electrical output.

The bias of the semiconductor laser was selected to achieve the best linearity in the specified input range while minimizing the power consumption. The optical link characteristics were tested by measuring the electrical output while applying a defined input.

| **Operational specifications** | **Min.** | **Typ.** | **Max.** | **Measured** |
|---|---|---|---|---|
| Total length [m] | 60 | 100 | 120 | 97 |
| Gain [V/V] | 0.25 | 0.8 | 2.5 | 2.08 (avg.) |
| Signal-to-noise ratio [dB] | | 48 | | 56.4 (avg.) |
| Integral linearity deviation [%] | | 2 | 4 | $< 0.5$ |
| Bandwidth [MHz] | 70 | | | 110 |
| Settling time to $\pm 1\%$ [ns] | | 18 | 20 | not measured |
| Skew [ns] | | | 2 | 0.25 |
| Jitter [ns] | | | 1 | 0.077 |
| Crosstalk [dB] | | -48 | | $< -57$ |

Table 5.9: Target specifications of the analog optical link compared to HEPHY measurements.

Tab. 5.9 gives an overview of the final specifications [69] and the HEPHY measurements, all of which are well within the specifications, although the prototype was designed with slightly different requirements: it had an electrical input range of $\pm 400$ mV (now $\pm 300$ mV) and a target gain of 2 V/V (now 0.8 V/V, leading to a higher noise figure). Details on the most important measurements are given below, while the full results can be obtained from [71].

As mentioned above, the bias was selected to get a linear input-output relation within the specified input range. The laser threshold can be visualized when exceeding this input range towards lower values. Fig. 5.46 shows the input-output characteristics of all four channels with a doubled input span. Towards the left edge, the laser threshold is exhibited, while at high input the receiver begins to saturate. Thus, nonlinearity occurs on either side of the nominal input window.

Fig. 5.47 shows the integral linearity deviation of the four channels, which is defined as the full-scale-normalized error one makes when, for a given link output signal y, the link input signal is assumed to be the linearized value instead of the real value.

The transfer function of the analog optical link was measured with an oscillator generating a sine wave of defined amplitude and frequency. The oscillator output was converted to a differential signal and sent into the optical link transmitter. Both input and output amplitudes were measured as a function of frequency, with their ratio defining the gain. From the transfer function (fig. 5.48), a $-3$ dB bandwidth of 110 MHz can be extracted. With this frequency response, the effect of transients on the APV output signal is negligible.

Apart from linearity, the noise figure, which is dominated by the laser contribution, plays an important role for the analog optical link. The output noise has been measured by the VME-ADC with an analog bandwidth 50 MHz and with a digital oscilloscope at several bandwidth

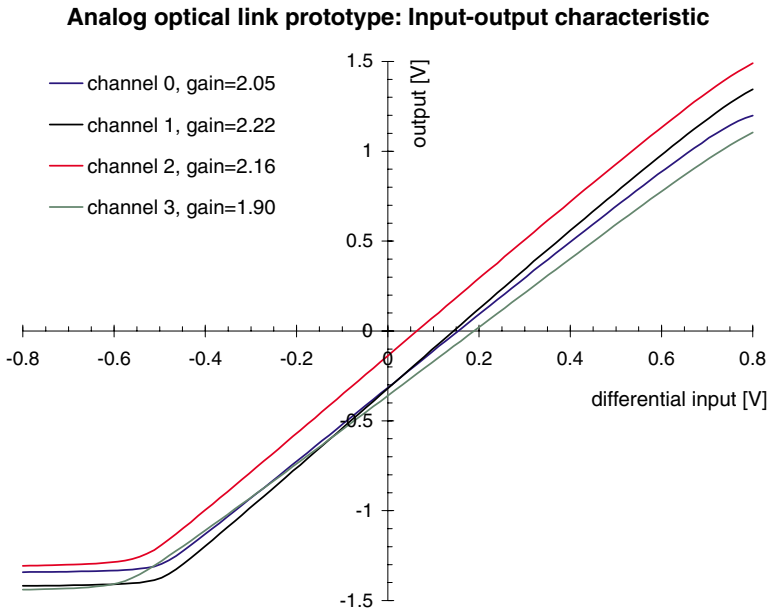



Figure 5.46: The input-output characteristics for all four channels of the analog optical link prototype. The nominal input span is in the linear range between $-400 \ldots +400\,\mathrm{mV}$.

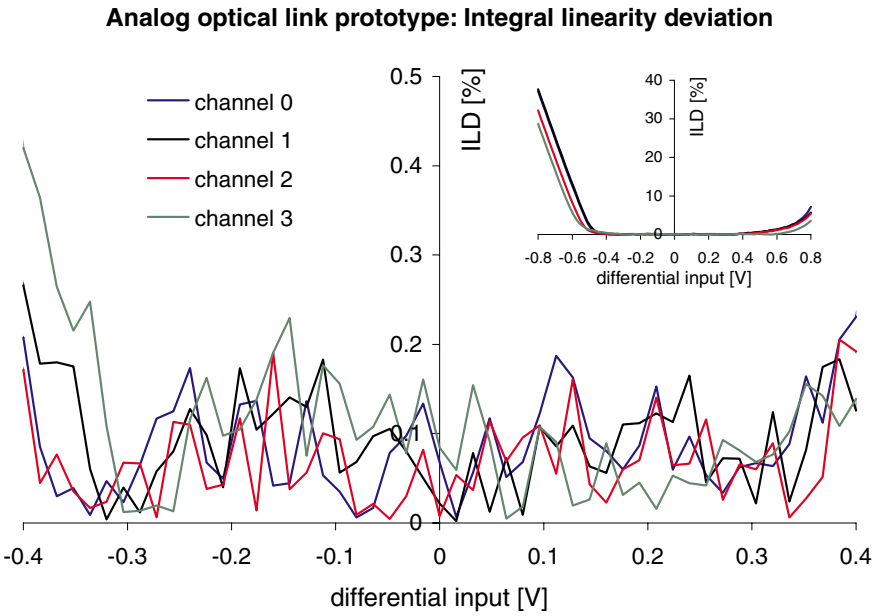



Figure 5.47: The integral linearity deviation of the analog optical link prototype. It remains below 0.5% within the nominal input span, but increases dramatically outside especially below the laser threshold, as shown in the insert.

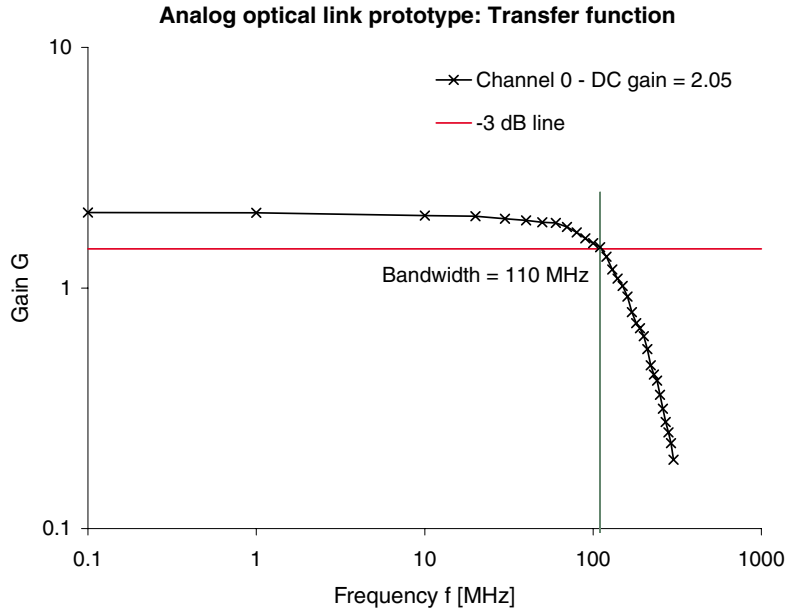



Figure 5.48: Transfer function of the analog optical link prototype. The bandwidth is the frequency where the amplification is 3 dB below the DC gain.

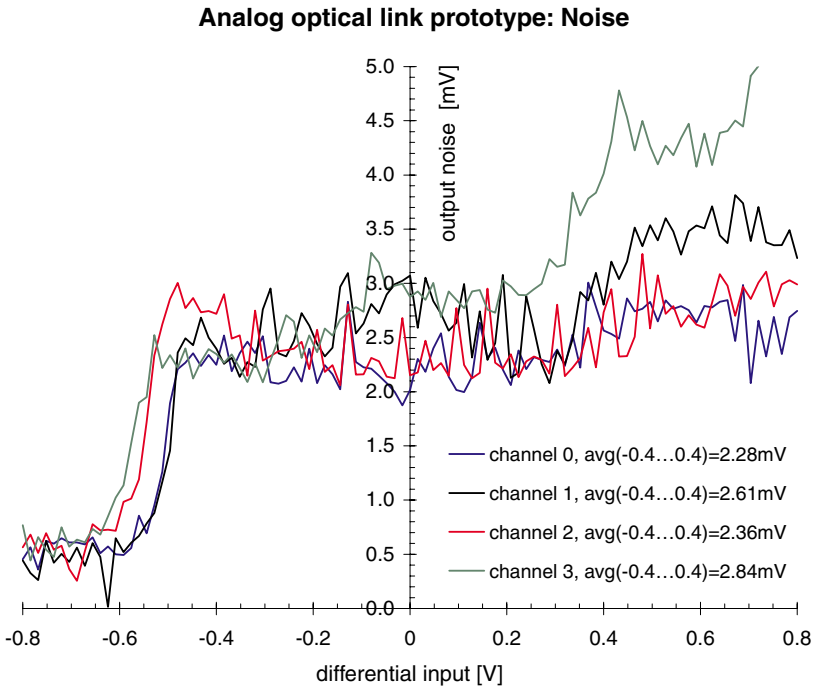



Figure 5.49: Noise of the analog optical link extrapolated to 500 MHz bandwidth.

limits. As the ADC measurement perfectly fits into the oscilloscope measurements, the ADC values have been scaled to represent the noise obtained at 500 MHz.

Fig. 5.49 shows the optical link noise vs. the input voltage, where the ADC noise is already subtracted. At the low edge, the optical output of the laser is zero, and thus the remaining noise (approximately 0.5 mV) is attributed to the receiver part. When the laser is turned on, its noise slightly increases with rising input voltage. The signal-to-noise ratio given in tab. 5.9 has been obtained by dividing the full range input span (800 mV) by the average noise referred to the input.

The noise of the analog optical link has been modelled and systematically studied with respect to device tolerances [70]. The measured noise behavior could be well reproduced by the model.

Apart from timing and crosstalk characteristics, the electrical power consumption of transmitter and receiver sections and the noise contribution in an APV6 system were measured. With the APV6, no difference in noise between copper cable and the optical link prototype could be observed, since the APV6 noise is quite high and the noise of the optical link prototype is lower than that of the final one due to the gain reduction. In the target system, using the APV25 and the final optical link, the latter will contribute approximately 600 e of noise referred to the APV input.

### 5.2.2 Laser Magnetic Field Test (March 2001)

This test was performed in collaboration with the CMS Tracker Optical Links group [72]. Two different types of semiconductor lasers were tested in the same magnetic field as the APV25S1 (see section 5.1.8, p. 110). Similar to the APV25, the lasers were also positioned in three orientations (A, B and C) as shown in fig. 5.50.

In this test, the lasers were driven by a programmable current source and optically connected to the analog optical link receiver hybrid. The voltage drop at the laser diode and the output of the analog receiver (level, linearity and noise) were measured as a function of the input current within the parameter space defined by laser type, orientation and magnetic field. Additionally, the optical output power and spectrum were analyzed.

Fig. 5.51 shows the optical output power of a typical semiconductor laser depending on the input current. Above a certain threshold, the light output power linearly increases with the input current. In this plot, the input current varies between zero and 100 mA, but only a small fraction of this range is used by the laser driver, which has a typical transconductance of 10 mS. Thus, the prototype analog optical link input span of 800 mV translates to a range of 8 mA. The bias is normally set close above the threshold, resulting in an operating range of the laser driver as shown in red.

A typical output spectrum of an edge-emitting semiconductor laser with a nominal wavelength of 1310 nm is shown in fig. 5.52. The lasing semiconductor is a narrow-band emitter of approximately Gaussian spectral shape enclosed in an optical resonator, consisting of two facing mirrors. One of the mirrors is semi-transparent to extract the light into the optical fiber. The optical resonator only leads to amplification when an integer multiple of half the wavelength fits in between the mirrors; other wavelengths are extinguished by destructive interference. This leads to the forked structure in the spectrum. The resonator condition for constructive interference is given by

$$N \frac{\lambda}{2} = D \quad , \tag{5.4}$$

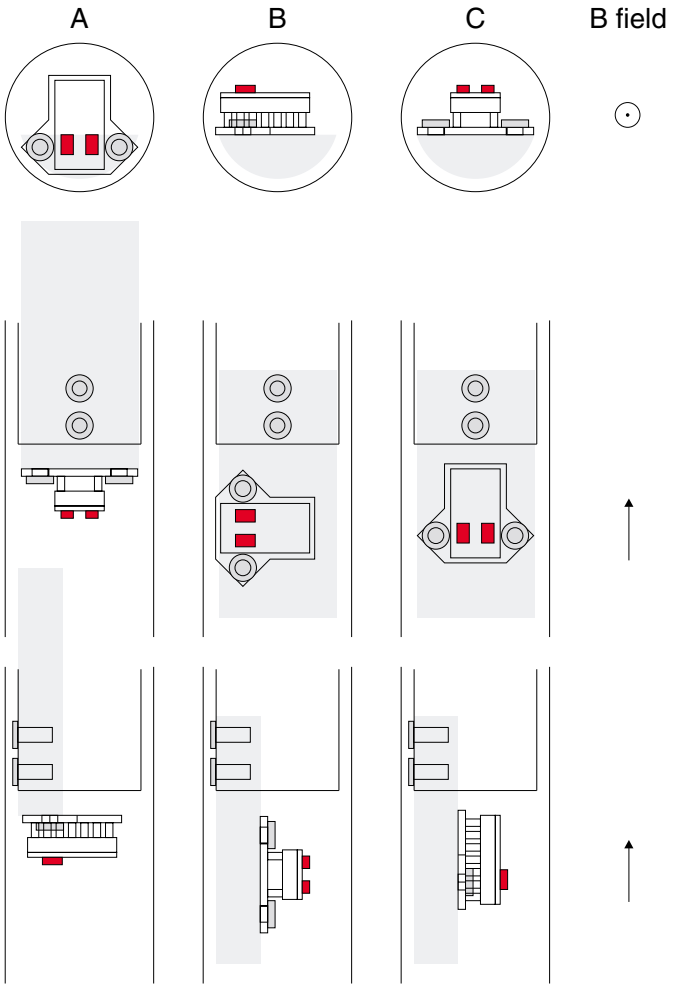



Figure 5.50: The three different orientations (A, B and C) of the semiconductor lasers (red) with respect to the magnetic field.

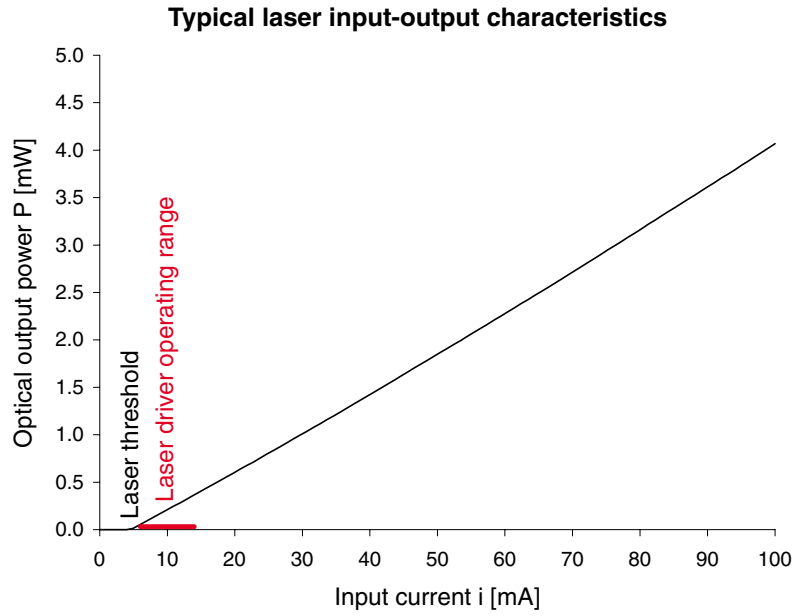



Figure 5.51: Typical laser output power vs. input current. The red bar represents the typical prototype laser driver output current range for its nominal input voltage span.

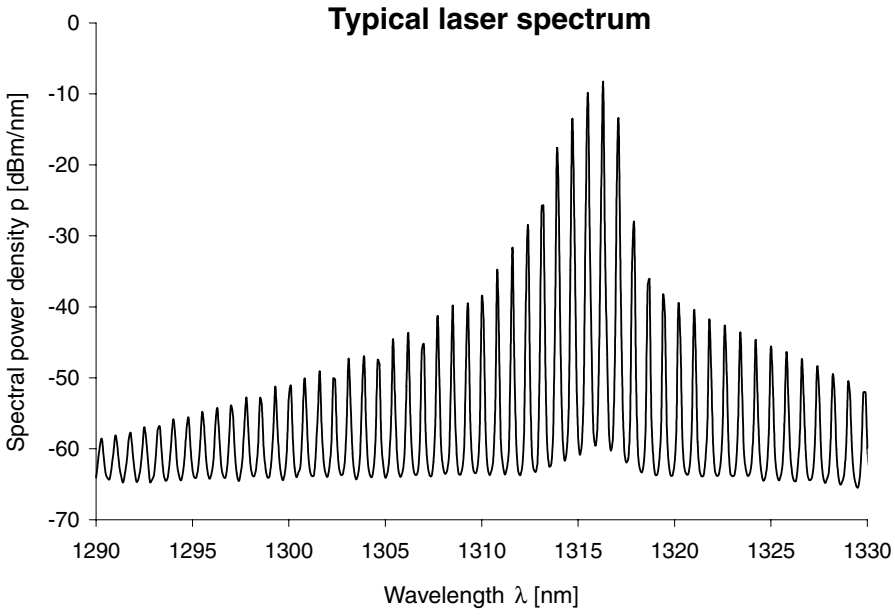



Figure 5.52: Typical output spectrum of an edge-emitting semiconductor laser with an input current of 15 mA.

with the wavelength $\lambda$, the resonator length $D$ and an integer multiple $N$. Knowing two neighboring spectral lines $\lambda_2 > \lambda_1$, the length of the optical resonator can be obtained by

$$D = \frac{1}{2\left(\lambda_1^{-1} - \lambda_2^{-1}\right)} \quad . \tag{5.5}$$

In the sample spectrum shown in fig. 5.52, the two highest adjacent peaks are found at $\lambda_1 = 1315.5\,\text{nm}$ and $\lambda_2 = 1316.3\,\text{nm}$. Eq. 5.5 returns a length of 1.08 mm for the optical resonator. The actual length is unknown, but all lasers tested for CMS have a resonator length about one millimeter.

It is obvious that the position of the spectrum peaks strongly depend on the actual length of the resonator. In fact, the method of interferometric length measurement employs this principle. When the laser is powered by a current flow, it slightly heats up compared to the zero current state. This causes the resonator to expand, resulting in a peak shift towards higher wavelengths. With an input current of 100 mA (corresponding to an electrical input power of approximately 176 mW), peak shifts in the order of 1 nA were observed, indicating a resonator expansion of approximately 1 $\mu$m.

The only effect observed in a precision scan of the magnetic field was a small shift in the laser threshold and slope. As shown in fig. 5.53, the laser threshold approximately depends on the square of the magnetic flux density, decreasing by about 4% at 10 T. The effect on the slope is even smaller. A relative change of less than 2% has been observed at the maximum magnetic field of 10 T.

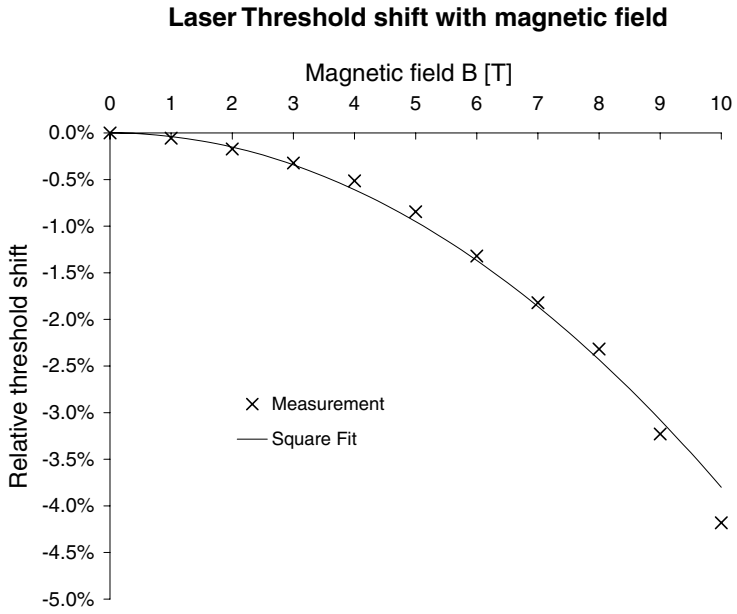



Figure 5.53: Dependence of the laser threshold of the magnetic field.

Thus, the influence of the magnetic field is very small. In fact, temperature effects largely dominate the performance of the laser, such that the presence of a magnetic field is irrelevant regarding the application in CMS. Not only the wavelength is affected by temperature, but also the input-output characteristics of the laser.

## 5.3 FED Evaluation (April 2001)

The analog behavior of the FED-PMC prototype was evaluated [73] with respect to the digitization of multiplexed APV data. The analog transfer characteristic of a digitizer is an important characteristic with respect to pulse distortion and noise sensitivity. Although clocked with the system frequency of 40 MHz, the analog input bandwidth for pulse digitization must be considerably higher to avoid signal loss due to slow transients.

The transfer function of the FED has been obtained by comparing the input from a sine wave generator to the digitized output. According to the sampling theorem by H.NYQUIST[2], analog information can only be truly reconstructed when sampled with at least twice the highest frequency contained in the analog data. If this condition is violated, aliasing effectively leads to "mirroring" of frequencies above half the sampling rate into the base band. Nevertheless, the amplitude of these signals reveal information about the analog performance.

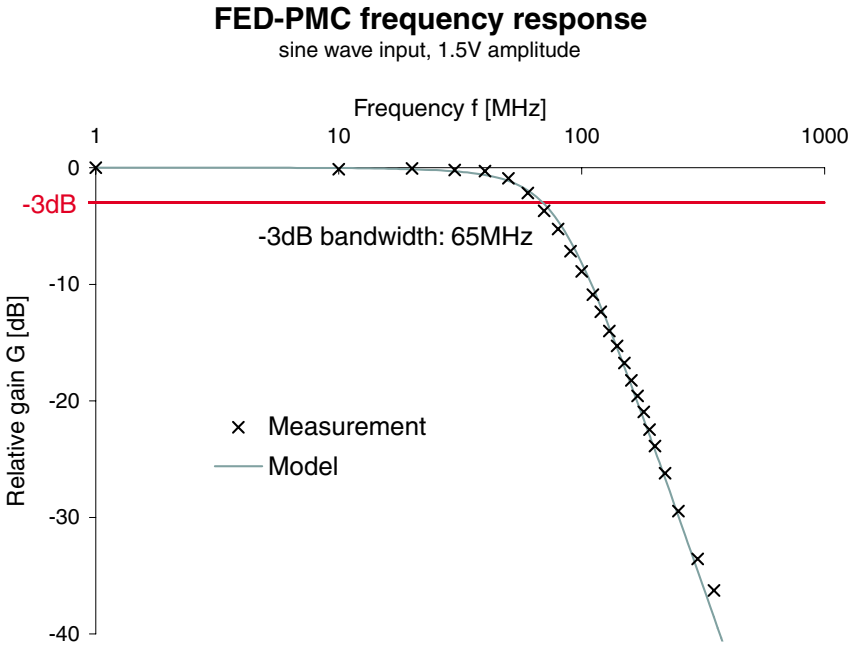



Figure 5.54: Transfer characteristic of the FED-PMC, measured with a sine wave input of 1.5 V amplitude (corresponding to the DC full range of the FED).

Fig. 5.54 shows the measured transfer function of the FED-PMC, normalized to the DC gain. A $-3$ dB bandwidth of 65 MHz has been extracted from these data. The transfer function has been modelled by a third-order system with two conjugated complex poles and one real pole. In terms of control theory, the model consists of a $PT_2$ element in series with a $PT_1$. Its transfer function in the Laplace plane is given by

$$G(s) = \frac{1}{\left(1 + \frac{s}{\omega_1}\right)\left(1 + \frac{2Ds}{\omega_n} + \frac{s^2}{\omega_n^2}\right)} \tag{5.6}$$

$$\text{with} \quad \omega_1 = \omega_n = 2\pi \cdot 80\,\text{MHz} \quad \text{and} \quad D = 0.6 \quad ,$$

[2] HARRY NYQUIST, *1889 in Nilsby (Sweden), †1976 in Harlingen, TX (USA). American physicist and electrical engineer who worked on the telegraph transmission theory.

where $\omega_1$ is the corner frequency of the $PT_1$, $\omega_n$ is the natural oscillation frequency and $D$ is the damping factor of the $PT_2$.

Moreover, the FED response to a rectangular input pulse with the width of one clock cycle was measured. Such a pulse emulates an APV channel with signal information, surrounded by pedestals. The response was measured by progressively delaying the input pulse relative to clock and trigger in steps of 1 ns, similar to the "sequential equivalent-time sampling" method [74] employed by some digital oscilloscopes. For comparison, the analytical transfer function model has been used to calculate the response to the same rectangular input pulse.

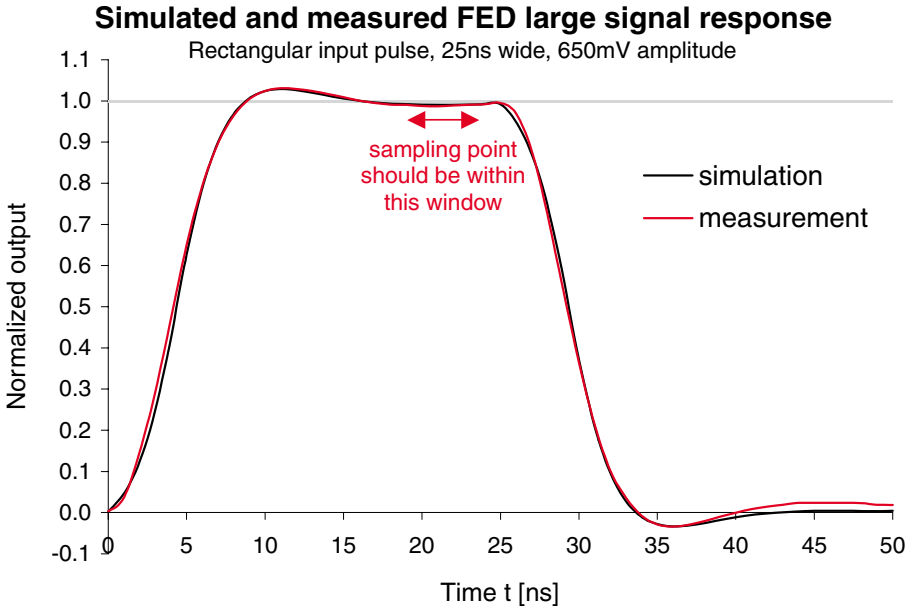



Figure 5.55: Normalized FED-PMC large signal response to an input pulse of 25 ns width and 650 mV amplitude.

Fig. 5.55 shows both measured and calculated FED responses to an input pulse of 25 ns width and an amplitude corresponding to 3.5 MIPs, assuming an APV25 input span of 8 MIPs projected onto the full FED input range. As seen from the matching curves, the model perfectly describes the system. An overshoot of less than 5% is the result of the damping factor being less than one, indicating a pair of complex poles. After the transients have vanished, a relatively flat period of about 5 ns occurs towards the end of the pulse. The actual sampling should be performed in the center of this span, allowing a certain jitter in the ADC clock.

The FED noise was measured by applying stable DC voltages to the FED input. Depending on the input voltage relative to an LSB step, we found a noise figure peaking at 0.5 ADC counts. This includes the digitization noise and the input amplifier to approximately equal parts. Using the nominal calibration of 1500 mV/512 ADC, the maximum noise contribution is 1.5 mV, referred to the input. With a full range of 8 MIPs, the noise figure corresponds to less than 175 e at the APV25 input.

Summarizing these results, the analog input stage of the FED reveals a bandwidth high enough to digitize the APV output without signal loss due to slow transients, while the FED noise contribution can be neglected compared to APV and optical link.

# Chapter 6

# Summary

The design of the CMS Silicon Strip Tracker and its electronic readout system has been presented in its specific environment. The n-type silicon detectors will be made of both 4" and 6" wafers with thicknesses of 300 and 500 $\mu$m, covering a total area of 206 m$^2$ with 10 million channels. The APV25 readout chip is a fast, low-noise, 128-channel charge sensitive amplifier with internal pipeline and deconvolution signal processing. In the front-end it is supported by several ASICs, which take over specific tasks in readout, control and monitoring. These chips include the APVMUX, which multiplexes the output of APV pairs onto a single line, the DCU, which monitors voltages, currents and temperatures, the PLL-Delay for providing clock and trigger signals and adjusting their phases, and the CCU, which handles control and monitoring signals. All CMS front-end chips will be manufactured in the radiation tolerant 0.25 $\mu$m deep submicron process. The control path between CCU in the front-end and FEC in the control room is connected with a digital optical link, while an analog optical link transmits the APV signals to the FED, where the data are digitized, processed and passed on to the event builder.

## 6.1 Silicon Detector Model

A simple model of charge collection in silicon detectors has been derived from the basics of semiconductor theory. It has been shown that the output signal of silicon detectors depends on various parameters like resistivity or bias voltage and approximately scales with the sensor thickness, thus demonstrating the feasibility of silicon detectors which are thicker than the canonical 300 $\mu$m. The APV amplifier in combination with the deconvolution method has also been implemented in the model.

## 6.2 APV Laboratory Tests

A powerful, yet flexible APV readout system and the related DAQ and analysis software were developed at the HEPHY, and numerous chips of APV6, APV25S0 and APV25S1 versions were tested. For the APV25S1 with no input load, equivalent noise charges of 267 and 425 e have been found in peak and deconvolution modes, respectively, agreeing with measurements by the chip developers. Moreover, an APVMUX switching time of less than 3 ns has been obtained together with negligible noise contribution.

## 6.3 Beam Tests

With control and monitoring tools to operate devices at the CMS Tracker design temperature of $-10°$ C, a cooling box was built. Three silicon detector modules were constructed at HEPHY including the very first modules with APV6 and APV25S0 readout. A typical MIP signal-to-noise ratio of 17 (corresponding to a noise of about 1300 e) has been obtained in beam tests for non-irradiated full-size CMS detector modules when read out by the APV25 in deconvolution mode, which outperforms the previous APV6 version especially in terms of noise. Pre-irradiated silicon detectors were included in these tests, showing a small but not critical degradation of the output signal. During a high-intensity beam period, a radiation induced leakage current increase of $\alpha \approx 8 \cdot 10^{-17}$ A cm$^{-1}$ was observed, which agrees with other measurements. Moreover, a prototype of the analog optical link was successfully tested in the module readout path.

The effects of radiation on both digital and analog sections of the APV25S1 circuitry were measured with 300 MeV/c pions. No permanent damage was observed, and a digital single event upset cross-section of approximately $2 \cdot 10^{-12}$ cm$^2$ has been found, which is compatible to similar measurements performed with heavy ions. From extrapolation of these data, a total upset rate in the order of 100 SEUs/hour is expected for Inner or Outer Barrel parts of the CMS Tracker. Analog upsets appear as a negligible increase in noise background.

## 6.4 Other Tests

The analog performance of optical link and FED was evaluated with very encouraging results. Their bandwidth is sufficiently high so that signals do not suffer from slow transients. Transfer characteristics, noise, linearity and other characteristics of the optical link were found to conform with their specifications. The final link will contribute about 600 e of noise referred to the APV input.

Both the APV25S1 and semiconductor lasers for the analog optical link have been tested in a magnetic field of up to 10 T. No effect on the APV chip was observed, while the lasers revealed small shifts of a few percent in threshold current and gain, which are negligible with respect to the application in the CMS Tracker.

## 6.5 Outlook

The results obtained from recent prototypes are quite solid and demonstrate the enormous progress that has been made in the CMS collaboration towards an optimum final system. While finishing the R&D phase, a gradual transition now takes place to the series construction of the CMS Silicon Strip Tracker components.

Approximately 600 silicon detector modules will be assembled and tested at HEPHY during the next years. Moreover, we will be responsible for design, production and testing of about 13000 analog optohybrids.

After the construction and installation phases, the CMS experiment will begin operation in 2006 and will hopefully deliver new physical results of high quality.

# Appendix A

# Acknowledgements

Many people at the HEPHY [1] and in the CMS Collaboration directly or indirectly contributed to the work described within this thesis.

First of all, I am indebted to DI Manfred Pernicka who is in charge of the Electronics II Group at the HEPHY. He constantly supported and advised me not only in electronic matters, but also e.g. in cross-country skiing. I also want to thank Doz. Manfred Krammer, head of the Semiconductor Detector Group at HEPHY, for sharing his knowledge about silicon detectors, the cooperative construction of detector modules and for advising this thesis. I am very grateful to my advisor Prof. Wolfgang Fallmann at the Vienna University of Technology, who also taught me the basics of semiconductors.

Furthermore, I want to acknowledge the prosperous teamwork with my colleague Thomas Bauer, who is an expert in optoelectronics. I would also like to thank Helmut Steininger and Siegfried Schmid of the Electronics II Group, who made the design and layout of numerous electronic modules, and Josef Pirker, who is extraordinarily talented in soldering almost invisible components. I want to express my thanks to our project leader Dr. Josef Hrubec for his support, to Dr. Rudi Wedenig and Margit Oberegger of the Semiconductor Detector Group for their professional skills in wire-bonding, and to Rudolf Eitelberger and Roland Stark of the Mechanics Workshop for their constructions.

Moreover, I want to emphasize the selfless support of Dr. Kurt Gabathuler and Dr. Dieter Renker with the $\pi$E1 and $\pi$M1 beamlines at PSI [65] and the help of Dr. Jonathan Fulcher of IC [75] with the single event upset measurements. I owe many thanks to the participants in the beam tests at PSI for the productive collaboration, to Prof. Geoff Hall at IC and Prof. Gigi Rolandi at CERN for promoting our tests and for "authorizing" this thesis, to Dr. Francois Vasey and his colleagues of the CMS Tracker Optical Links group [72] for their continuous support with optoelectronics and to Prof. Wolfgang Lang of IMP [68] for providing the superconducting magnet.

Last but not least I am very grateful to my girlfriend Michaela Liebhart for her patience while I was working on this thesis and for proofreading. This task was also performed by my parents Hedy and Friedrich Friedl, whom I wish to express my big thanks also for their mental support and interest in my work.

# Appendix B

# Abbreviations and Symbols

The list below explains abbreviations used in this thesis.

| Abbreviation | Meaning (explanation) |
|---|---|
| AC | Alternating Current |
| ADC | Analog-to-Digital Converter |
| APSP | Analog Pulse Shape Processor |
| APV | (CMS silicon strip tracker amplifier chip series) |
| APVMUX | APV Multiplexer |
| ASIC | Application Specific Integrated Circuit |
| ALICE | A Large Ion Collider Experiment (LHC experiment, `http://www.cern.ch/ALICE`) |
| ATLAS | A Toroidal LHC Apparatus (LHC experiment, `http://atlasinfo.cern.ch/Atlas`) |
| BNL | Brookhaven National Laboratory, Upton, USA (`http://www.bnl.gov`) |
| bx | Bunch Crossing |
| CCU | Communications and Control Unit |
| CERN | European Laboratory for Particle Physics, Geneva, CH [2] (`http://www.cern.ch`) |
| CMC | Common Mode Correction |
| CMOS | Complementary Metal-Oxide Semiconductor |
| CMS | Compact Muon Solenoid (LHC experiment, `http://cmsinfo.cern.ch/cmsinfo`) |
| CP | Charge-Parity |
| CRT | Cathode Ray Tube (monitor) |
| CSC | Cathode Strip Chambers |
| DELPHI | Detector with Lepton, Photon and Hadron Identification (LEP experiment) |
| DAC | Digital-to-analog converter |
| DAQ | Data Acquisition |
| DC | Direct Current |
| DCU | Detector Control Unit |
| DLL | Delay-Locked Loop |
| DMILL | (Radiation hard ASIC manufacturing process by Temic) |
| DPM | Dual Port Memory |
| DT | Drift Tube Chambers |

*continued on next page*

*continued from previous page*

| Abbreviation | Meaning (explanation) |
|---|---|
| ECAL | Electromagnetic Calorimeter |
| FEC | Front-End Controller |
| FET | Field Effect Transistor |
| FIFO | First In First Out (memory) |
| FOXFET | Field Oxide Field Effect Transistor |
| FPGA | Field Programmable Gate Array |
| FWHM | Full Width at Half Maximum |
| GUI | Graphical User Interface |
| HCAL | Hadron Calorimeter |
| HEPHY | Institute of High Energy Physics, Vienna, A [1] (`http://wwwhephy.oeaw.ac.at`) |
| HV | High Voltage |
| $I^2C$ | Inter-IC (bus system) |
| IC | Integrated Circuit |
| | Imperial College, London, UK [75] (`http://www.hep.ph.ic.ac.uk/silicon`) |
| IMP | Institute of Material Physics, Vienna, A [68] |
| | (`http://www.univie.ac.at/materialphysik`) |
| LEP | Large Electron Positron Collider |
| LHC | Large Hadron Collider (`http://www.cern.ch/LHC`) |
| LHCb | (B-meson experiment at LHC, `http://lhcb.cern.ch`) |
| LVDS | Low Voltage Differential Signaling |
| MIP | Minimum Ionizing Particle |
| MIT | Massachusetts Institute of Technology, Cambridge, USA (`http://www.mit.edu`) |
| MQW | Multi-Quantum-Well (semiconductor laser structure) |
| MSGC | Micro-Strip Gas Chamber |
| MUX | Multiplexer |
| NIM | Nuclear Instrumentation Module |
| NOMAD-STAR | Neutrino Oscillation Magnetic Detector - Silicon Target |
| | (`http://nomadinfo.cern.ch/`) |
| NRZI | Non Return to Zero with Invert 1 on change (Data encoding scheme) |
| NTC | Negative Temperature Coefficient |
| PC | Personal Computer |
| PCB | Printed Circuit Board |
| PCI | Peripheral Component Interconnect (Industrial bus system) |
| PHOBOS | (RHIC Experiment, `http://phobos-srv.chm.bnl.gov`) |
| PLL | Phase-Locked Loop |
| PM | Photomultiplier (tube) |
| PMC | PCI Mezzanine Card |
| ppm | Parts Per Million |
| PSI | Paul Scherrer Institute, Villigen, CH [65] (`http://www.psi.ch`) |
| PUC | Pixel Unit Cell |
| R&D | Research & Development |
| RHIC | Relativistic Heavy Ion Collider (`http://www.rhic.bnl.gov`) |
| ROOT | (Object-oriented data analysis software package [61], `http://root.cern.ch`) |
| RMS | Root Mean Square |
| RPC | Resistive Plate Chambers |

*continued on next page*

*continued from previous page*

| Abbreviation | Meaning (explanation) |
|---|---|
| SEGR | Single Event Gate Rupture |
| SEL | Single Event Latchup |
| SEU | Single Event Upset |
| S/H | Sample/Hold |
| SM | Standard Model |
| SMS | Short Message Service |
| SNR | Signal-to-Noise Ratio |
| SPICE | Simulation Program with Integrated Circuit Emphasis (Circuit Simulation Software) |
| SPS | Super Proton Synchrotron (CERN accelerator) |
| SST | Silicon Strip Tracker |
| SUSY | Supersymmetry |
| TTC | Timing, Trigger and Control (LHC clock and trigger distribution system [58]) |
| VCO | Voltage Controlled Oscillator |
| VFT | Very Forward Tracker |
| VME | Versa Module Eurocard (Industrial bus system) |

This list defines the symbols used for variables and constants.

| Symbol | Definition | Units or Value |
|---|---|---|
| $\alpha$ | Current related damage rate | $\mathrm{A/m}$ |
| | Tilt angle | $^\circ$ |
| $\beta$ | Speed relative to $c$ | |
| $\delta(\gamma)$ | Density correction term | |
| $\epsilon$ | Dielectric constant | $\mathrm{A\,s\,V^{-1}\,m^{-1}}$ |
| $\eta$ | Pseudorapidity | |
| $\eta_c$ | Charge collection efficiency | |
| $\gamma$ | $(1-\beta^2)^{-1/2}$ | |
| $\lambda$ | Wavelength | $\mathrm{m}$ |
| $\lambda_I$ | Nuclear interaction length | $\mathrm{m}$ |
| $\mu$ | Carrier mobility | $\mathrm{m^2\,V^{-1}\,s^{-1}}$ |
| $\Phi$ | fluence | $\mathrm{m^{-2}}$ |
| $\Phi_{\mathrm{eq}}$ | 1 MeV neutron equivalent fluence | $\mathrm{m^{-2}}$ |
| $\rho$ | Mass density | $\mathrm{kg\,m^{-3}}$ |
| | Charge density | $\mathrm{e\,m^{-3}}$ |
| $\sigma$ | Standard deviation | *any unit* |
| | Cross-section | $\mathrm{m^2}$ |
| $A$ | Atomic mass | kg/mol |
| | Amplifier gain | |
| | Scale factor | |
| $B$ | Magnetic flux density | T |
| $c$ | Speed of light in vacuum | $3.00 \cdot 10^8\,\mathrm{m/s}$ |
| $C$ | Capacitance | F |
| | Shell correction term | |

*continued on next page*

*continued from previous page*

| Symbol | Definition | Units or Value |
|---|---|---|
| clw | Cluster width | |
| $D$ | Detector thickness | m |
| | Optical resonator length | m |
| $d_c$ | Charge collection distance | m |
| $E$ | Electric field strength | V/m |
| | Energy | eV |
| $e$ | Elementary charge | $1.60 \cdot 10^{-19}$ A s |
| $E_g$ | Band gap | eV |
| ENC | Equivalent noise charge | e |
| $f$ | Frequency | Hz |
| $i$ | Current | A |
| $I$ | Mean excitation energy | eV |
| $k$ | Boltzmann constant | $8.62 \cdot 10^{-5}$ eV/K |
| $L$ | Field effect transistor channel length | m |
| $\mathcal{L}$ | Luminosity | $\mathrm{m}^{-2}\,\mathrm{s}^{-1}$ |
| $m_e$ | Electron mass | $9.11 \cdot 10^{-31}$ kg |
| $n$ | Number of electron-hole pairs | |
| $N$ | Doping concentration density | $\mathrm{m}^{-3}$ |
| $n, N$ | Integer multiple | |
| $N_A$ | Avogadro constant | $6.02 \cdot 10^{23}\,\mathrm{mol}^{-1}$ |
| $p$ | Particle momentum | eV/c |
| | Strip pitch | m |
| $Q$ | Charge | e |
| $Q_c$ | Collected charge | e |
| $r$ | Radius | m |
| | Resistivity | $\Omega$ m |
| $R$ | Event rate | $\mathrm{s}^{-1}$ |
| $r_e$ | Classical electron radius $\frac{e^2}{4\pi\epsilon_0 m_e c^2}$ | 2.82 fm |
| SNR | Signal-to-noise ratio | |
| $T$ | Absolute temperature | K |
| $t, T$ | Time | s |
| $T_{\max}$ | Maximum kinetic energy transfer | eV |
| $T_p$ | Peaking time | s |
| $v$ | Velocity | m/s |
| $V$ | Voltage | V |
| | Volume | $\mathrm{m}^3$ |
| $W$ | Field effect transistor channel width | m |
| $w$ | Strip implant width | m |
| $x$ | Distance from the detector backplane | m |
| $X_0$ | Radiation length | m |
| $z$ | Distance from the vertex along the beam axis | m |
| | Particle charge relative to $e$ | |
| $Z$ | Atomic Number | |

# Appendix C

# Bibliography


[1] Austrian Academy of Sciences, Institute of High Energy Physics, Nikolsdorfergasse 18, A-1050 Vienna, Austria (`http://wwwhephy.oeaw.ac.at`)

[2] European Laboratory for Particle Physics, CH-1211 Geneva 23, Switzerland (`http://www.cern.ch`)

[3] Particle Data Group, **Particle Physics Booklet**, Springer, July 2000 (`http://pdg.lbl.gov`)

[4] S.Cittolin, **Introduction to CMS**, CMS Brochure, March 1988 (`http://cmsinfo.cern.ch/Brochures/IntroToCMS.pdf`)

[5] C.E.Wulz (CMS Collaboration), **CMS - Concept and Physics Potential**, CMS CR-1999/012, March 1999 (`http://cmsdoc.cern.ch/cgi-doc/Grep/documents/all.html?_GEN_`)

[6] T.S.Virdee (CMS Collaboration), **The CMS Experiment at the LHC**, CMS CR-1998/025, January 1999 (`http://cmsdoc.cern.ch/cgi-doc/Grep/documents/all.html?_GEN_`)

[7] CMS Collaboration, **CMS Tracker Technical Design Report**, CERN/LHCC 98-6, April 1998 (`http://cmsdoc.cern.ch/cms/TDR/TRACKER/tracker.html`)

[8] CMS Collaboration, **Addendum to the CMS Tracker TDR**, CERN/LHCC 2000-016, February 2000 (`http://cmsdoc.cern.ch/cms/TDR/TRACKER/tracker_addendum.pdf`)

[9] M.Winkler, **dE/dx in Halbleiterdetektoren**, Diploma Thesis, Vienna University of Technology, September 1998

[10] L.D.Landau, **On the Energy Loss of Fast Particles by Ionization**, Collected Papers of L.D.Landau, Pergamon Press, Oxford, 1965

[11] C.Ede, **Messung der Energiedeposition von geladenen Teilchen in dünnen Siliziumdetektoren**, Diploma Thesis, Vienna University of Technology, December 1999

[12] M.Friedl, **PSI-Testbeam December 2000** (`http://cern.ch/friedl` → PSI-Testbeam)

[13] P. Shulek *et al.*, **Fluctuations of Ionization Losses** Soviet Journal of Nuclear Physics 4 (1967), 400

[14] M.S.Tyagi, **Introduction to Semiconductor Materials and Devices**, John Wiley & Sons, 1991

[15] S.M.Sze, **Semiconductor Devices**, John Wiley & Sons, 1985

[16] S.Ramo, **Currents Induced by Electron Motion**, Proceedings of the I.R.E. 27 (1939), 584-585

[17] CERN RD42 Collaboration - Diamond Detectors (`http://cern.ch/rd42`)

[18] CERN RD8 Collaboration - GaAs Detectors (`http://ppewww.ph.gla.ac.uk/RD8`)

[19] M.Friedl, T.Bauer, M.Krammer, **A Simple Model of Charge Collection in Silicon Detectors**, Nuclear Instruments and Methods in Physics Research A 461 (2001), 192-196

[20] T.Bauer, M.Friedl, **Silicon Detector Simulation** (`http://cern.ch/bauer/sim`)

[21] Tabularized NIEL values compiled from several publications are available at `http://sesam.desy.de/~gunnar`

[22] Rose Collaboration (RD48), **Third RD48 Status Report**, CERN/LHCC 2000-009, December 1999 (`http://cern.ch/rd48`)

[23] H.Pernegger, **The Silicon Ministrip Detector of the DELPHI Very Forward Tracker**, PhD Thesis, Vienna University of Technology, February 1996

[24] G.Baricchello *et al.*, **Performance of Long Modules of Silicon Microstrip Detectors**, CERN-PPE 97-162, December 1997 (`http://nomadinfo.cern.ch/Public/detect/star/publications.html`)

[25] S.Braibant *et al.*, **Investigation of design parameters and choice of substrate resistivity and crystal orientation for the CMS silicon microstrip detector**, CMS NOTE 2000/056 (`http://cmsdoc.cern.ch/documents/00/note00_011.pdf`)

[26] H.Pernegger (PHOBOS Collaboration), **Layout and tests of silicon pad detectors for the PHOBOS experiment at RHIC**, Nuclear Instruments and Methods in Physics Research A 419 (1998), 549-555

[27] B.Back *et al.*, **The PHOBOS Silicon Pad Sensors**, Nuclear Instruments and Methods in Physics Research A 447 (2000), 257-263

[28] Y.Gornushkin *et al.*, **Monolithic Active Pixel Sensors for Charged Particle Tracking**, 9th Vienna Conference on Instrumentation, Vienna, A, February 2001 (`http://wwwhephy.oeaw.ac.at/u3w/w/wcc/www/talks/Thursday/Dulinski.pdf`)

[29] W.de Boer *et al.*, **Lorentz angle measurements in irradiated silicon detectors between 77 and 300 K**, Nuclear Instruments and Methods in Physics Research A 461 (2001), 200-203

[30] A.Rudge, **Comparison of Charge Collection in Semiconductor Detectors and Timing Resolution, Using a Sub-Nanosecond Transimpedance Amplifier**, Nuclear Instruments and Methods in Physics Research A 360 (1995), 169-176

[31] E. Nygård *et al.*, **CMOS Low Noise Amplifier for Microstrip Readout: Design and Results**, Nuclear Instruments and Methods in Physics Research A 301 (1991), 506-516

[32] S.Gadomski *et al.*, **The Deconvolution Method of Fast Pulse Shaping at Hadron Colliders**, Nuclear Instruments and Methods in Physics Research A 320 (1992), 217-227

[33] N.Bingefors *et al.*, **A novel technique for fast pulse-shaping using a slow amplifier at LHC**, Nuclear Instruments and Methods in Physics Research A 326 (1993), 112-119

[34] J.D.Schipper, **Low-Noise Preamplifier** (`http://www.nikhef.nl/~jds/vlsi`)

[35] M.Raymond *et al.*, **Measurements of transistors and silicon microstrip detector readout circuits in the Harris AVLSIRA rad-hard CMOS process**, Nuclear Instruments and Methods in Physics Research A 351 (1994), 449-459

[36] TEMIC Semiconductors, MHS S.A., La Chantrerie - Route de Gachet, B.P. 70602, F-44306 Nantes Cedex 3, France (`http://www.temic-semi.com`)

[37] Information on the IBM 0.25 $\mu$m process can be found at `http://www.chips.ibm.com/services/foundry/offerings/cmos/6sf`

[38] A.Duccio, **The Tracker Layout** (`http://cern.ch/duccio/layout/whole.html`)

[39] R.Baur, W.Bertl, **The CMS Pixel Vertex Detector**, Nuclear Physics B, Proc. Suppl.: 78 (1999), 293-300

[40] K.Gabathuler, **CMS Pixel Readout Electronics**, International Pixel Detector Workshop – Pixel 98, Batavia, IL, USA, FERMILAB-Conf-98-196, 171-178 (`http://fnalpubs.fnal.gov/archive/1998/conf/Conf-98-196.html`)

[41] R.Baur, **Readout Architecture of the CMS Pixel Detector**, International Pixel Detector Workshop – Pixel 2000, Genova, Italy, submitted to Nuclear Instruments and Methods in Physics Research A

[42] **Supply of Silicon Micro-Strip Sensors for The CMS Silicon Strip Tracker (SST)**, Invitation to Tender/Technical Specification, CERN/IT-2777/EP/CMS, October 2000 (`http://cern.ch/angarano/sensors/specifications.pdf`)

[43] M.Lenzi (CMS Tracker Collaboration), **Performance of the all-silicon CMS Tracker**, November 2000, submitted to Nuclear Instruments and Methods in Physics Research A

[44] R.Wedenig (CMS Tracker Collaboration), **Assembly Studies for Silicon Detector Modules**, 9th Vienna Conference on Instrumentation, Vienna, A, February 2001 (submitted to Nuclear Instruments and Methods in Physics Research A)

[45] Information on the Philips $I^2C$ bus (including specifications) can be found at `http://www.semiconductors.philips.com/i2c`

[46] M.Raymond, **APV25-S0 Analogue Test Results**, December 1999 (available at `http://www.te.rl.ac.uk/med/apv25_web/APV25_talk.pdf`)

[47] M.Raymond *et al.*, **The APV6 Readout Chip for CMS Microstrip Detectors**, CERN/LHCC 97-60, September 1997 (`http://www.te.rl.ac.uk/med/apv6/papers/leb_apv6_london97_paper.pdf`)

[48] R.Turchetta *et al.*, **Design and results from the APV25, a Deep Submicron CMOS Front-End Chip for the CMS Tracker**, 4th International Symposium on Development and Application of Semiconductor Tracking Detectors, Hiroshima, Japan, March 2000 (`http://www.te.rl.ac.uk/med/apv25_web/hiroshima00_slides.pdf`)

[49] L.L.Jones *et al.*, **The APV25 Deep Submicron Chip for CMS Detectors**, CERN/LHCC 99-09, p.162-166, September 1999 (`http://www.te.rl.ac.uk/med/apv25_web/leb99_paper.pdf`)

[50] G.Marseguerra, **Prestazioni del chip di lettura APV25 dei rivelatori a microstrip su silicio del tracker di CMS**, PhD Thesis, July 2000 (`http://pcigor2.pd.infn.it/APV_25/giorgio/Main.ps.gz`)

[51] Information and Manuals of the Microelectronics Design Group, Instrumentation Department, Rutherford Appleton Laboratory, are available at `http://www.te.rl.ac.uk/med`

[52] Z.Y.Chang, W.M.C.Sansen, **Low-Noise Wide Band Amplifiers in Bipolar and CMOS Technologies**, Kluwer Academic Publishers, Boston, November 1990

[53] A.Neviani, **APV25S0 - Calibration Circuit** (`http://www.te.rl.ac.uk/med/apv25_web/cal.pdf`)

[54] CMS Tracker Control (`http://pcvlsi5.cern.ch/CMSTControl`)

[55] G.Cervelli *et al.*, **Radiation Tolerant Linear Laser Driver IC** (`http://cern.ch/cms-tk-opto/technical.html`)

[56] F.Faccio *et al.*, **An 80Mbit/s radiation tolerant Optical Receiver for the CMS digital optical link** (`http://cern.ch/cms-tk-opto/dev_pubs.html`)

[57] T.Bauer, **Digital Optical Link** (`http://cern.ch/bauer/opto.html`)

[58] CERN RD12 Collaboration - Timing, Trigger and Control (TTC) Systems for LHC Detectors (`http://cern.ch/TTC/intro.html`)

[59] J.Coughlan, **The CMS Tracker Front-End Driver (FED)** (`http://hepwww.rl.ac.uk/cms_fed`)

[60] Information about the cooling box developed at HEPHY and the MultiTherm temperature monitoring system can be found at `http://cern.ch/friedl`

[61] ROOT – An Object-Oriented Data Analysis Framework (`http://root.cern.ch`)

[62] M.Friedl, **APV6 Vienna Manual** (`http://cern.ch/friedl` → APV6)

[63] W.Adam *et al.*, **Response of a silicon detector to protons and pions with momenta of 270, 310 and 405 MeV/c**, Nuclear Instruments and Methods in Physics Research A 441 (2000), 427-437

[64] M.Raymond *et al.*, **The CMS Tracker APV25 0.25 $\mu$m CMOS Readout Chip**, CERN/LHCC 2000-41, p.130-134, September 2000 (`http://cern.ch/lebwshop/LEB00_Book/tracker/raymond.pdf`)

[65] Paul Scherrer Institute, CH-5232 Villigen, Switzerland (`http://www.psi.ch`)

[66] J.Fulcher *et al.*, **Single Event Upset Studies on the APV25 Front End Readout Chip**, CERN/LHCC 2000-41, p.260-264, September 2000 (`http://cern.ch/lebwshop/LEB00_Book/rad/fulcher.pdf`)

[67] M.Friedl, **Strasbourg FE Hybrid Test** (`http://cern.ch/friedl` → APV25)

[68] Vienna University, Institute of Material Physics, High Temperature Superconductivity Group, Kopernikusgasse 15, A-1060 Vienna, Austria (`http://www.univie.ac.at/materialphysik`)

[69] F.Vasey *et al.*, **CMS Tracker Optical Readout Link Specification**, Part 1: Analog Readout System (`http://cern.ch/cms-tk-opto/specifications.html`)

[70] T.Bauer, F.Vasey, **A model for the CMS tracker analog optical link**, CMS NOTE 2000/056 (`http://cern.ch/cms-tk-opto/perf_pubs.html`)

[71] T.Bauer, M.Friedl, **Optical Link Evaluation** (`http://cern.ch/friedl` → AOL)

[72] F.Vasey *et al.*, **CMS Tracker Optical Links** (`http://cern.ch/cms-tk-opto`)

[73] M.Friedl, **Analog Performance of the FED-PMC** (`http://cern.ch/friedl` → FED)

[74] Tektronix Technique Primer 47W-7209, **Sampling Oscilloscope Techniques** (`http://www.tektronix.com/Measurement/App_Notes/sampling_primer`)

[75] Imperial College, High Energy Physics, Silicon Group, Blackett Laboratory, Prince Consort Road, London SW7 2BZ, United Kingdom (`http://www.hep.ph.ic.ac.uk/silicon`)

# Appendix D

# Curriculum Vitae

Markus Friedl
Belvederegasse 19/8
A-1040 Vienna
Austria

Markus.Friedl@cern.ch
http://cern.ch/friedl

I was born on July 18, 1973 in Vienna, Austria and still live there. After kindergarten, I attended primary school from 1979 until 1983, followed by BRG 12 Rosasgasse (grammar school) where I graduated in 1991 with honors. In spring 1991, I placed 6th at the Austrian Physics Olympiad.

Between 1989 and 1994, I had several summer jobs with Siemens, IBM, Honeywell and Shell. The majority of these jobs dealt with administrative projects and computer programming.

From 1991 on, I have been studying Electrical Engineering at the Vienna University of Technology. In January 1999, I made my diploma exam (MEng) with honors and decided to head for the doctoral degree, which is completed by this thesis.

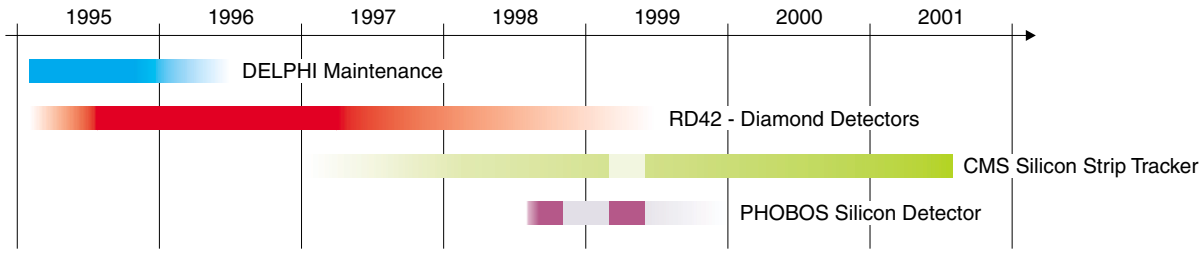
Since 1995, I have been working with the Institute of High Energy Physics of the Austrian Academy of Sciences. I began with maintenance jobs on gas detectors of the DELPHI experiment at CERN (CH), but soon switched over to Diamond Detector research as a member of the CERN RD42 collaboration, which was also the topic of my Diploma Thesis. Already in 1998, I commenced my work on the CMS Silicon Strip Tracker, interrupted by a temporary employment at MIT and BNL (both USA) in early 1999, where I took part in the construction of the Silicon Spectrometer of the PHOBOS Experiment.

For the near future, I intend to stay with the HEPHY at least during the CMS construction period.

A more detailed and up-to-date CV is available at `http://cern.ch/friedl` → CV.

## D.1 List of Experiments

The graph below summarizes my occupation in the field of high energy physics. Only the CMS related work is covered by this thesis. Research on diamond detectors was already the topic of my diploma thesis.




The list below gives an overview of the measurements discussed within this thesis. I was participating in all tests as a member of HEPHY, and in most cases, I was the leading experimenter.

| **Date** | **Location** | **Description** | Reference |
|---:|:---:|---|---|
| July 1997 | PSI | Prototype CMS detector beam test at low energies and various incident angles | [63] |
| June 1998 | CERN | Multiregion CMS detector beam test with APV6 readout | section 5.1.3, p. 81 |
| October 1998 | BNL | Precise energy loss measurements on PHOBOS silicon pad detector modules | fig. 2.2, p.16, and [11] |
| September 1999 | HEPHY | Analog optical link evaluation | section 5.2.1, p. 113 |
| 2000/2001 | HEPHY | Several APV25 laboratory tests | section 5.1.4, p. 85 |
| May/December 2000 | PSI | Extensive CMS silicon detector module tests with APV6 and APV25 readout | section 5.1.5, p. 88 |
| December 2000 | PSI | APV25 irradiation tests | section 5.1.6, p. 99 |
| February 2001 | HEPHY | APVMUX laboratory tests | section 5.1.7, p. 107 |
| March 2001 | IMP | Magnetic field tests on APV25 and analog optical link | section 5.1.8, p. 110, and section 5.2.2, p. 116 |
| April 2001 | HEPHY | FED analog performance evaluation | section 5.3, p. 120 |

The results of the tests associated with CMS were presented in numerous collaboration meetings at CERN.

## D.2 List of Publications

M.Friedl, **Diamond Detectors for Ionizing Radiation**, Diploma Thesis, University of Technology, Vienna, January 1999 (`http://cern.ch/friedl`)

M.Friedl *et al.*, **CVD Diamond Detectors for Ionizing Radiation**, Nuclear Instruments and Methods in Physics Research A 435 (1999), 194-201

W.Adam *et al.*, **Response of a silicon detector to protons and pions with momenta of 270, 310 and 405 MeV/c**, Nuclear Instruments and Methods in Physics Research A 441 (2000), 427-437

M.Friedl, T.Bauer, M.Krammer, **A Simple Model of Charge Collection in Silicon Detectors**, Nuclear Instruments and Methods in Physics Research A 461 (2001), 192-196

Co-author of several RD42, PHOBOS and CMS collaboration publications

Web: `http://cern.ch/friedl`

Articles about the Vienna APV25 module and the single event upset measurements are in preparation and will be submitted for publication.